example, extends 0.4 microns below surface 9 of die 8. A source contact 17 is placed on surface 9 in electrical contact with body region 12 and a source contact region portion of source region 13. A drain contact 19 is placed on surface 9 in electrical contact with drain contact region 16. An insulating layer 7 is placed on surface 9 of die 8. A gate contact 18 is placed on insulating layer 7 over a channel region portion of body region 12, as shown.

Between body region 12 and region 16 is a region 14 of second conductivity type. Region 14 is, for example, n-type material doped at 2 x 10^{12} atoms per square centimeter. Region 14 extends downward from surface 9 to a depth of, for example 0.4 microns. Located below region 14 is a region 15 of first conductivity type. Region 15 is, for example, p-type material doped at 4 x 10^{12} atoms per square centimeter. Region 15 extends from surface 9 downward a depth of, for example 1 micron. Region 15 is connected to ground at surface 9 in a plane not shown in Figure 1. A distance 6 between and edge of body region 12 and an edge of drain contact 16 is, for example 12 microns. A symmetry line 20 is used for placing a second half of the transistor in a mirror image to the first half shown in Figure 1.

The circuit shown in Figure 1, may also function as a bipolar transistor with region 13 functioning as an emitter, region 12 functioning as a base, and pocket 11, region 14 and region 16 functioning as an extended collector.

Figure 2 shows a circuit diagram for the lateral double-diffused insulated gate field effect transistor with an

extended drain region which is a parallel combination of a single-sided JFET and a double-sided JFET shown in Figure 1. A transistor 22 is controlled by gate contact 18. Current through transistor 22 travels from source contact 17 through region 13 through body region 12 to region 11, shown in Figure 1.

The extended drain region of transistor 22 includes a single-sided JFET 24 and a double-sided JFET 21 connected in parallel as shown. Current through single-sided JFET 24 passes through region 14 and through region 16 to drain contact 19. Region 15 serves as the single side of single-sided JFET 24. Current through double-sided JFET 21 passes through region 11 and through region 16 to drain contact 19. Region 15 and substrate 10 serve as the two sides of double-sided JFET 21.

The above-discussed design allows for significant reduction of resistance from source contact 17 to drain contact 19 when transistor 22 is "on", over circuits in the prior art. The present invention is also simpler to manufacture than related prior art devices.

Figure 3 shows a cross-sectional view of a lateral double-diffused insulated gate field effect transistor with extended drain region in accordance with an alternate preferred embodiment of the present invention. The transistor shown in Figure 3 is surrounded by isolation diffusion which is necessary in order to isolate the transistor from other devices on an integrated circuit.

A substrate 110 of first conductivity type is, for example, made of p^--type material doped with 5×10^{14} atoms per cubic centimeter. A typical depth of substrate 110 is 500 microns. A layer 111 of material of second conductivity type is, for example, n-type epitaxial material doped at 10^{15} atoms per cubic centimeter. Layer 111 extends a depth of, for example, 10 to 25 microns below a surface 109.

For a first half of the transistor, a body region 112 of first conductivity type is, for example, p-type material doped at between 10^{17} and 10^{20} atoms per cubic centimeter. Body region 112 typically extends a depth of 1 micron below surface 109. Within body region 112, a source region 113 of second conductivity type is, for example, n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Source region 113, for example, extends 0.4 microns below surface 109.

A drain contact region 116 of second conductivity type is, for example, n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Drain contact region 116, for example, extends 0.4 microns below surface 109.

A source contact 117 is placed on surface 109 in electrical contact with body region 112 and a source contact region portion of source region 113. A drain contact 119 is placed on surface 109 in electrical contact with drain contact region 116. An insulating layer 107 is placed on surface 109. A gate contact 118 is placed on insulating layer 107 over a channel region portion of body region 112, as shown.

Between body region 112 and region 116 is a region 114 of second conductivity type. Region 114 is, for example, n-type material doped at 2 x 10^{12} atoms per square centimeter. Region 114 extends downward from surface 109 to a depth of, for example 0.4 microns. Located below region 114 is a region 115 of first conductivity type. Region 115 is, for example, p-type material doped at 4 x 10^{12} atoms per square centimeter. Region 115 extends from surface 109 downward a depth of, for example 1 micron. Region 115 is connected to ground at surface 109 in a plane not shown in Figure 1.

A second half of the transistor is a mirror image of the first half of the transistor with symmetry around drain contact region 116. For the second half of the transistor, a body region 132 of first conductivity type is, for example, p-type material. Within body region 132, a source region 133 of second conductivity type is, for example, n^+-type material.

A source contact 137 is placed on surface 109 adjacent to body region 132 and in electrical contact with source region 133. A gate contact 138 is placed on insulating layer 107 over a channel region portion of body region 132, as shown.

Between body region 132 and region 116 is a region 134 of second conductivity type. Region 134 is, for example, n-type material. Located below region 134 is a region 135 of first conductivity type. Region 135 is connected to ground at surface 109 in a plane not shown in Figure 3.

The transistor shown in Figure 3, may also function as a bipolar transistor with region 113 and region 133 functioning as an emitter, region 112 and region 132 functioning as a

base, and layer 111, region 114, region 134 and region 116 functioning as an extended collector.

An isolation region 141, an isolation region 142, an isolation region 143 and an isolation region 144, each of first conductivity type, provide isolation for the transistor from other devices. Isolation regions 141 through 144 are, for example, of p-type material doped at between 10^{16} and 10^{19} atoms per cubic centimeter. Isolation region 141 and isolation region 143 are diffused down while isolation region 142 and isolation region 144 are diffused up.

When a device is either embedded in a well or an epitaxial layer, a severe problem can arise when the diode formed by the body region and the well (or epitaxial layer) is forward biased and the diode formed by the well region and the substrate is backed biased at a high negative voltage (e.g., less than -50 volts). Specifically, this can trigger a parasitic bipolar transistor where the body region will act as an emitter, the well (or epitaxial layer) will act as base and the substrate will act as a collector. The gain of such a parasitic bipolar transistor is typically more than 100; therefore, practically all the current will flow to the substrate creating a parasitic power dissipation through the substrate. To solve this issue, a layer of semiconductor material of opposite conductivity type from the conductivity type of the substrate may be buried under the well (or epitaxial layer) to drastically reduce the gain of the parasitic bipolar transistor. In many cases even this scheme does not result in sufficient isolation for optimal

performance. In such cases, the isolation scheme shown in Figure 4 may be utilized.

Figure 4 shows a cross-sectional view of two lateral double-diffused insulated gate field effect transistors with extended drain regions where the transistors are additionally shielded from the substrate and other devices.

A substrate 210 of first conductivity type is, for example, made of p^--type material doped with 5×10^{14} atoms per cubic centimeter. A typical depth of substrate 210 is 500 microns. A layer 211 of material of second conductivity type is, for example, n-type epitaxial material doped at 10^{15} atoms per cubic centimeter. Layer 211 extends a depth of, for example, 12 to 17 microns below a surface 209.

For a first half of the transistor, a body region 212 of first conductivity type is, for example, p-type material doped at between 10^{17} and 10^{20} atoms per square centimeter. Body region 212 typically extends a depth of 1 micron below surface 209. Within body region 212, a source region 213 of second conductivity type is, for example, n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Source region 213, for example, extends 0.4 microns below surface 209.

A drain contact region 216 of second conductivity type is, for example, n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Drain contact region 216, for example, extends 0.4 microns below surface 209.

A source contact 217 is placed on surface 209 in electrical contact with body region 212 and a source contact

region portion portion of source region 213. A drain contact 219 is placed on surface 209 in electrical contact with drain contact region 216. An insulating layer 207 is placed on surface 209. A gate contact 218 is placed on insulating layer 207 over a channel region portion of body region 212, as shown.

Between body region 212 and region 216 is a region 214 of second conductivity type. Region 214 is, for example, n-type material doped at 2 x 10^{12} atoms per square centimeter. Region 214 extends downward from surface 209 to a depth of, for example 0.4 microns. Located below region 214 is a region 215 of first conductivity type. Region 215 is, for example, p-type material doped at 4 x 10^{12} atoms per square centimeter. Region 215 extends from surface 209 downward a depth of, for example 1 micron. Region 215 is connected to ground at surface 209 in a plane not shown in Figure 1.

A second half of the transistor is a mirror image of the first half of the transistor with symmetry around drain contact region 216. For the second half of the transistor, a body region 232 of first conductivity type is, for example, p-type material. Within body region 232, a source region 233 of second conductivity type is, for example, n^+-type material.

A source contact 237 is placed on surface 209 adjacent to body region 232 and in electrical contact with source region 233. A gate contact 238 is placed on insulating layer 207 over a channel region portion of body region 232, as shown.

Between body region 232 and region 216 is a region 234 of second conductivity type. Region 234 is, for example, n-type

material. Located below region 234 is a region 235 of first conductivity type. Region 235 is connected to ground at surface 209 in a plane not shown in Figure 4.

The transistor shown in Figure 4, may also function as a bipolar transistor with region 213 and region 233 functioning as an emitter, region 212 and region 232 functioning as a base, and layer 211, region 214, region 234 and region 216 functioning as an extended collector.

Isolation layers and isolation regions isolate the transistor from the substrate and from other devices. Surrounding the transistor shown in Figure 4 is an isolation region 241, an isolation region 243 and an isolation region 250. Additionally, an isolation region 266 and an isolation region 267 are adjacent to a region 254 of epitaxial material of the second conductivity type. An isolation region 268 and an isolation region 269 are adjacent to a region 255 of epitaxial material of the second conductivity type. Additionally a sinker region 251 and a sinker region 253 are located as shown.

Isolation region 241, isolation region 243, isolation region 250, isolation region 266, isolation region 267, isolation region 268 and isolation region 269 are each of first conductivity type, for example, p-type material doped at between 10^{16} and 10^{20} atoms per cubic centimeter. Sinker region 251 and sinker region 253 are, for example of n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Region 254 and region 255 are, for example, of n

type epitaxial material doped at 10^{15} atoms per cubic centimeter.

In addition to Isolation region 250, a buried layer 249 of second conductivity type is placed to provide further isolation of the transistor from substrate 210. Buried layer 249 consists of, for example, n^+-type semiconductor material doped at between 10^{17} and 10^{19} atoms per cubic centimeter. Region 250 has a depth 261 of, for example, three microns. Buried layer 249 has a depth 262 of, for example, ten microns. Region 250 and buried layer 249 combine to effectively isolate substrate 210 from the transistor device even at high voltages.

Figure 5 shows another shielding arrangement which isolates devices used in high voltage applications. A substrate 310 of first conductivity type is, for example, made of p^--type material doped with 5×10^{14} atoms per cubic centimeter. A typical depth of substrate 210 is 500 microns. A layer 350 of material of first conductivity type is, for example, p-type epitaxial material doped at between 5×10^{15} and 5×10^{16} atoms per cubic centimeter. Layer 350 extends a depth of, for example, 10 to 25 microns below a surface 309.

Active devices are placed within a well 311 of second conductivity type. Well 311 is, for example, n-type material doped at 5×10^{15} and 5×10^{16} atoms per cubic centimeter. Well 311 extends a depth of, for example, 5 microns below a surface 309.

Isolation layers and isolation regions isolate a device within well 311 from substrate 310 and from other devices.

Immediately below well 311 is a region 351 which is part of layer 350. Surrounding well 311 and region 351 is an isolation region 341, and an isolation region 342. Surrounding isolation region 341 and isolation region 342 are a sinker region 331 and a sinker region 332.

Isolation region 341 and isolation region 342 are each of first conductivity type, for example, p^+-type material doped at between 10^{17} and 10^{19} atoms per cubic centimeter. Sinker region 331 and sinker region 332 are, for example of n^+-type material doped at between 10^{17} and 10^{19} atoms per cubic centimeter.

A buried layer 349 of second conductivity type is placed to provide isolation of the device in well 311 from substrate 310. Buried layer 349 consists of, for example, n^+-type semiconductor material doped at between 10^{17} and 10^{19} atoms per cubic centimeter. Buried layer 349 has a depth of, for example, ten microns. Region 351 and buried layer 349 combine to effectively isolate substrate 310 from the device in well 311 even at high voltages greater than 50 volts.

The foregoing discussion discloses and describes merely exemplary methods and embodiments of the present invention. For example, in the above discussion the first conductivity type is n-type material and the second conductivity type is p-type material. Alternately, the first conductivity type could be p-type material and the second conductivity type could be n-type material. As will be understood by those familiar with the art, the invention may be embodied in other specific forms without departing from the spirit or essential

characteristics thereof. Accordingly, the disclosure of the present invention is intended to be illustrative, but not limiting, of the scope of the invention, which is set forth in the following claims.

Claims

I Claim:

1. A semiconductor device comprising:

a substrate of first conductivity type;

a pocket of semiconductor material of second conductivity type which adjoins a surface of the substrate;

a body region of semiconductor material of the first conductivity type which is within the pocket of semiconductor material and which adjoins the surface of the substrate;

a source region of semiconductor material of the second conductivity type, the source region being within the body region and adjoining the surface of the substrate;

a drain contact region of semiconductor material of the second conductivity type within the pocket of semiconductor material which adjoins the surface of the substrate;

a first intermediate region of semiconductor material of the first conductivity type which adjoins the surface of the substrate and which is located within the pocket of semiconductor material between the body region and the drain contact region; and,

a second intermediate region of semiconductor material of the second conductivity type which adjoins the surface of the substrate and which is located within the pocket of semiconductor material between the body region and the drain contact region, wherein a portion of the second intermediate region extends between the first intermediate region and the surface of the substrate.

2. A semiconductor device as in claim 1 wherein the substrate is electrically coupled to the body region by extending a portion of the the body region out of the pocket of semiconductor material.

3. A semiconductor device as in claim 1 wherein the semiconductor device is a lateral double-diffused insulated gate field effect transistor with an extended drain region.

4. A semiconductor device as in claim 1 wherein the semiconductor device is a bipolar transistor, the source region functioning as an emitter, and the body region functioning as a base.

5. A semiconductor device comprising:

a drain contact;

a single-sided JFET having a first end electrically coupled to the drain contact and having a second end;

a double-sided JFET having a first end electrically coupled to the first end of the single-sided JFET and having a second end electrically coupled to the second end of the single-sided JFET;

a source contact;

a gate contact;

an insulated gate field effect transistor having a gate region coupled to the gate contact, having a source region electrically coupled to the source contact, and having a drain

region electrically coupled to the second end of the single-sided JFET and to the second end of the double-sided JFET.

6. A semiconductor device as in claim 5 wherein the double-sided JFET comprises:

a first semiconductive path within a pocket of semiconductor material of second conductivity type, the pocket of semiconductor material being within a substrate of first conductivity type, wherein a first region of semiconductor material of first conductivity type is placed between the first semiconductive path and a surface of the substrate.

7. A semiconductor device as in claim 6 wherein the single-sided JFET comprises:

a second semiconductive path composed of semiconductor material of second conductivity type; the second semiconductive path residing between the first region of semiconductor material and the surface of the substrate.

8. A semiconductor device as in claim 7 wherein the insulated gate field effect transistor comprises:

a body region of semiconductor material of the first conductivity type, the body region being within the pocket of semiconductor material wherein the body region adjoins the surface of the substrate and is separated from the gate contact by a layer of insulator placed on the surface of the substrate; and,

a source region of semiconductor material of the second conductivity type, the source region being within the body region and the source region being electrically coupled to the source contact.

9. A semiconductor device as in claim 5 wherein the double-sided JFET comprises:

a first semiconductive path within a layer of epitaxial material of second conductivity type, the layer of epitaxial material being deposited on a substrate of first conductivity type, wherein a first region of semiconductor material of first conductivity type is placed between the first semiconductive path and a surface of the layer of epitaxial material.

10. A semiconductor device as in claim 9 wherein the single-sided JFET comprises:

a second semiconductive path composed of semiconductor material of second conductivity type; the second semiconductive path residing between the first region of semiconductor material and the surface of the layer of epitaxial material.

11. A semiconductor device as in claim 10 wherein the insulated gate field effect transistor comprises:

a body region of semiconductor material of the first conductivity type, the body region being within the layer of epitaxial material wherein the body region adjoins the surface

of the layer of epitaxial material and is separated from the gate contact by a layer of insulator placed on the surface of the layer of epitaxial material; and,

a source region of semiconductor material of the second conductivity type, the source region being within the body region and the source region being electrically coupled to the source contact.

12. A semiconductor device comprising:

a substrate of first conductivity type;

a layer of epitaxial material of second conductivity type deposited on a surface of the substrate;

a body region of semiconductor material of the first conductivity type which is within the layer of epitaxial material and which adjoins the surface of the layer of epitaxial material;

a source region of semiconductor material of the second conductivity type, the second contact region being within the body region and adjoining the surface of the layer of epitaxial material;

a drain contact region of semiconductor material of the second conductivity type within the layer of epitaxial material which adjoins the surface of the layer of epitaxial material;

a first intermediate region of semiconductor material of the first conductivity type which adjoins the surface of the layer of epitaxial material and which is located within the

Claims 12-22

layer of epitaxial material between the body region and the drain contact region; and,

a second intermediate region of semiconductor material which adjoins the surface of the layer of epitaxial material and which is located within the layer of epitaxial material between the body region and the drain contact region, wherein a portion of the second intermediate region extends between the first intermediate region and the surface of the layer of epitaxial material.

13. A semiconductor device as in claim 12 wherein the semiconductor device is isolated from other semiconductor devices within the substrate by isolation layers of the first conductivity type within the layer of epitaxial material.

14. A semiconductor device as in claim 13 wherein the semiconductor device is isolated from the substrate by a first isolation layer of the first conductivity type diffused within the layer of epitaxial material, and by a buried layer of the second conductivity layer diffused within the layer of epitaxial material and below the first isolation layer.

15. A semiconductor device as in claim 12 wherein the semiconductor device is a lateral double-diffused insulated gate field effect transistor with an extended drain region.

16. A semiconductor device as in claim 12 wherein the semiconductor device is a bipolar transistor, the source

region functioning as an emitter, and the body region functioning as a base.

17. A semiconductor device comprising:

a substrate of first conductivity type;

a layer of epitaxial material of second conductivity type deposited on a surface of the substrate;

a body region of semiconductor material of the first conductivity type which is within the layer of epitaxial material and which adjoins the surface of the layer of epitaxial material;

a source region of semiconductor material of the second conductivity type, the second contact region being within the body region and adjoining the surface of the layer of epitaxial material;

a drain contact region of semiconductor material of the second conductivity type within the layer of epitaxial material which adjoins the surface of the layer of epitaxial material;

a first isolation layer of the first conductivity type diffused in the layer of epitaxial material; and,

a buried layer of the second conductivity layer diffused in the layer of epitaxial material and below the first isolation layer.

18. A semiconductor device as in claim 17 additionally comprising:

a first intermediate region of semiconductor material of the first conductivity type which adjoins the surface of the layer of epitaxial material and which is located within the layer of epitaxial material between the body region and the drain contact region; and,

a second intermediate region of semiconductor material of second conductivity type which adjoins the surface of the layer of epitaxial material and which is located within the layer of epitaxial material between the body region and the drain contact region, wherein a portion of the second intermediate region extends between the first intermediate region and the surface of the layer of epitaxial material.

Sub 94

19. Shielding for a high power semiconductor device, the high power semiconductor device being placed in a layer of epitaxial material of second conductivity type deposited on a surface of a substrate of first conductivity type, the shielding comprising:

an isolation layer of the first conductivity type diffused in the layer of epitaxial material;

a first isolation region within the layer of epitaxial material and surrounding the high power semiconductor device, the first isolation region extending from the surface of the layer of epitaxial material to the isolation layer and the first isolation region being of the first conductivity type;

a buried layer of the second conductivity layer diffused into the layer of epitaxial material and below the first isolation layer;

a second isolation regions surrounding the first isolation region, the second isolation region extending from the surface of the layer of epitaxial material to the buried layer and the second isolation region being of the second conductivity type;

an epitaxial region surrounding the second isolation region, the epitaxial region extending from the surface of the layer of epitaxial material to a depth below the second isolation region; and,

a third isolation region surrounding the epitaxial region, the third isolation region extending from the surface of the layer of epitaxial material and the third isolation region being of the first conductivity type.

20. A semiconductor device as in claim 17 wherein the semiconductor device is a lateral double-diffused insulated gate field effect transistor with an extended drain region.

21. A semiconductor device as in claim 17 wherein the semiconductor device is a bipolar transistor, the source region functioning as an emitter, and the body region functioning as a base.

22. A shielding for a high power semiconductor device within a layer of epitaxial material of first conductivity type deposited on a substrate of the first conductivity type, the shielding comprising:

a well of second conductivity type which adjoins a surface of the layer of epitaxial material, the high power semiconductor device being placed in the well;

a buried layer of the second conductivity layer diffused into the layer of epitaxial material;

an isolation region of first conductivity type, within the layer of epitaxial material located above the buried layer and surrounding the well; and,

a sinker region of second conductivity type, placed above the buried layer and surrounding the isolation region.

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Abstract of the Disclosure

An insulated gate field effect transistor with an extended drain region is presented. The extended drain region includes a single-sided JFET and a double-sided JFET connected in parallel. The insulated gate field effect transistor is built on a substrate of first conductivity type. A pocket of semiconductor material of second conductivity type is within the substrate adjoining a surface of the substrate. A body region of semiconductor material of the first conductivity type is within the pocket adjoining the surface of the substrate. Also, a source region of semiconductor material of the second conductivity type is within the body region adjoining the surface of the substrate. A drain contact region of semiconductor material of the second conductivity type is also within the pocket of semiconductor material adjoining the surface of the substrate. A first intermediate region of semiconductor material of the first conductivity type is within the pocket of semiconductor material between the body region and the drain contact region. The first intermediate region adjoins the surface of the substrate. Also, a second intermediate region of semiconductor material of second conductivity type is within the pocket of semiconductor material between the body region and the drain contact region. The second intermediate region also adjoins the surface of the substrate. A portion of the second intermediate region extends between the first intermediate region and the surface of the substrate.

PATENT APPLICATION

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION ATTORNEY DOCKET NO. 1003-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: DEVICE WHICH FUNCTIONS AS A LATERAL DOUBLE-DIFFUSED INSULATED GATE FIELD EFFECT TRANSISTOR OR AS A BIPOLAR TRANSISTOR

the specification of which

[X] is attached hereto.
[ ] was filed on _____ as Application Serial No. _____
[ ] was amended by the preliminary amendment filed with the original application papers.

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above and that I have disclosed the best mode for carrying out the invention as of the filing date of the application. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

[ ] In compliance with this duty there is attached an information disclosure statement 37 CFR 1.97.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: ___ NO: ___
			YES: ___ NO: ___
			YES: ___ NO: ___

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the attorney(s) and/or agent(s) listed below to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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602 836 Fremont St.
701 Santa Clara, CA 95050
(408) 985-0642

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Klas H. Eklund 40100 Citizenship: Finland

Residence/Post Office Address: 103 Los Patios, Los Gatos, CA 95030 CA

Inventor's Signature _____ Date 8/9/91

(Use Page Two For Additional Inventor(s) Signature(s))

Rev 5/90 (Form 3.02)

FCS1685987

Patent

Applicant: KLAS H. EKLUND Attorney's Docket Number: 1003
For: DEVICE WHICH FUNCTIONS AS A LATERAL DOUBLE-DIFFUSED INSULATED GATE FIELD EFFECT TRANSISTOR OR AS A BIPOLAR TRANSISTOR

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.27(b)) - INDEPENDENT INVENTOR

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9 (c) for purposes of paying fees under section 41(a) and (b) of Title 35, United States Code with regard to the invention entitled: DEVICE WHICH FUNCTIONS AS A LATERAL DOUBLE-DIFFUSED INSULATED GATE FIELD EFFECT TRANSISTOR OR AS A BIPOLAR TRANSISTOR described in the specification filed herewith.

I have not assigned, granted conveyed or licensed and am under no obligation under contract or law to assign, grant convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9 (c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey or license any rights in the invention is listed below.

--POWER INTEGRATIONS, INC., 411 Clyde Ave, Mtn. View, CA 94043.

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: KLAS H. EKLUND
Address of Person Signing: 103 Los Patios, Los Gatos, CA 95030

Signature: _____

Date: 8/9/91

Print or Drawings
As Originally Filed

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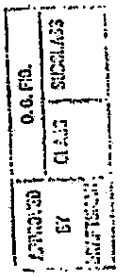

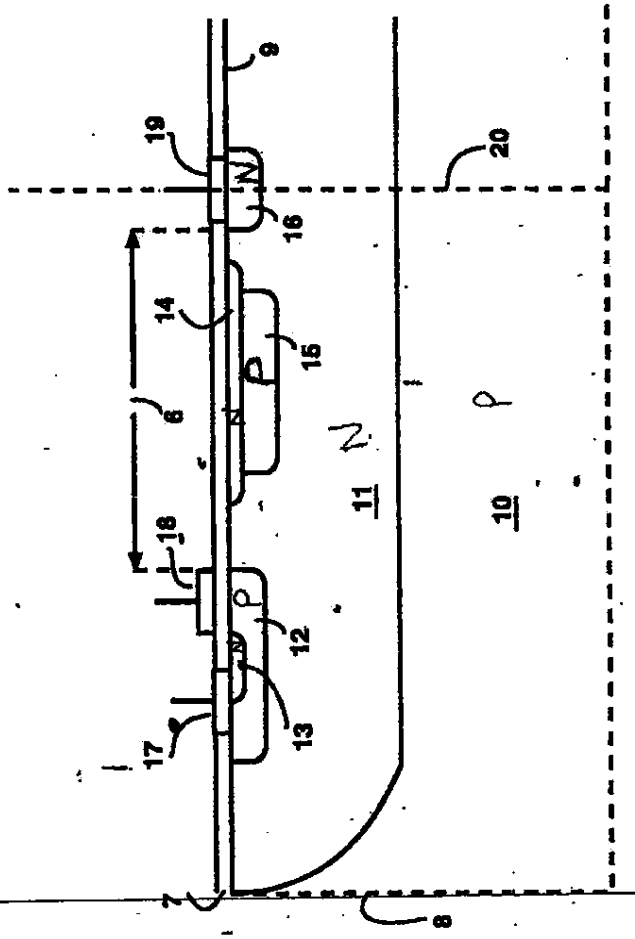

FIG. 1

Print Of Drawings
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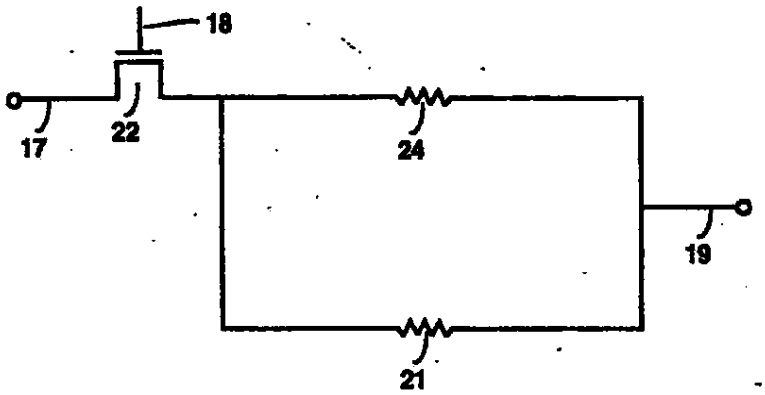

FIG. 2

Print of Drawings
As Originally Filed

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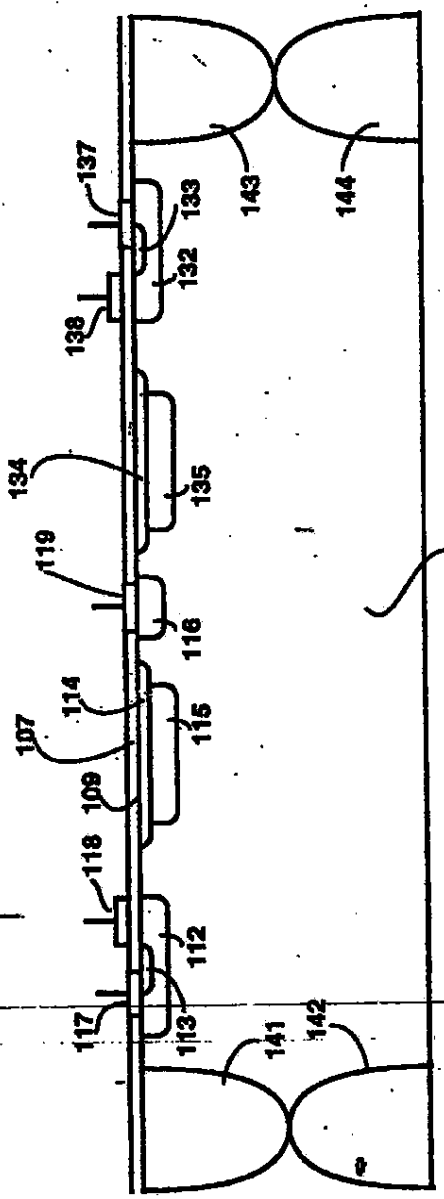

FIG. 3

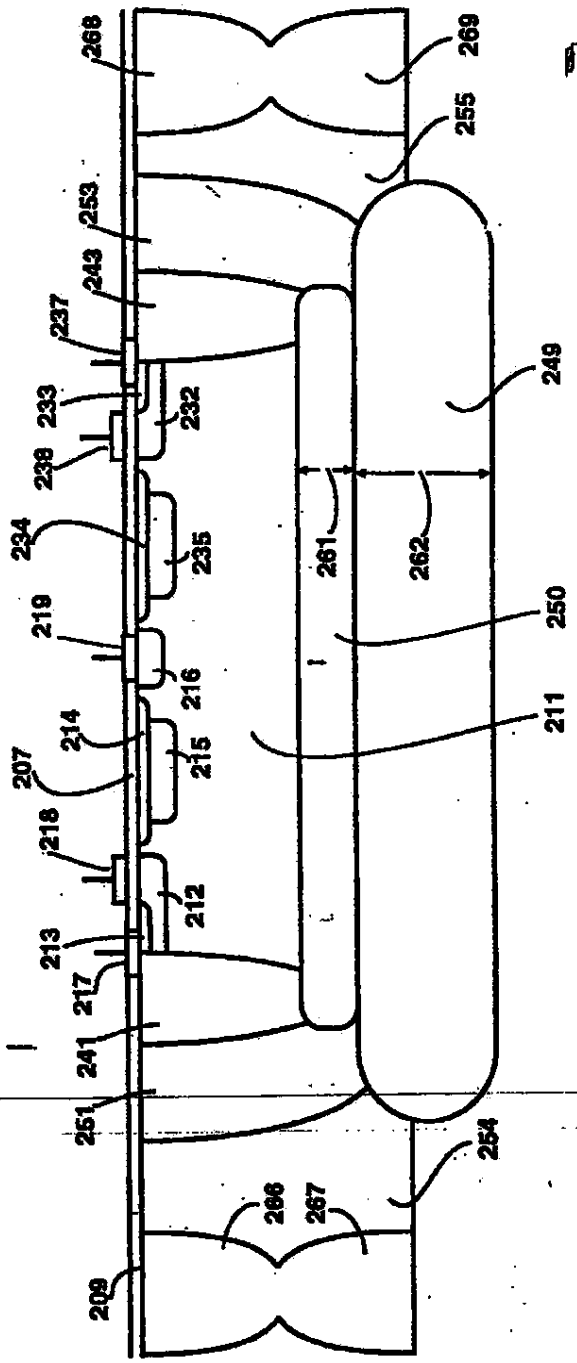

FIG. 4

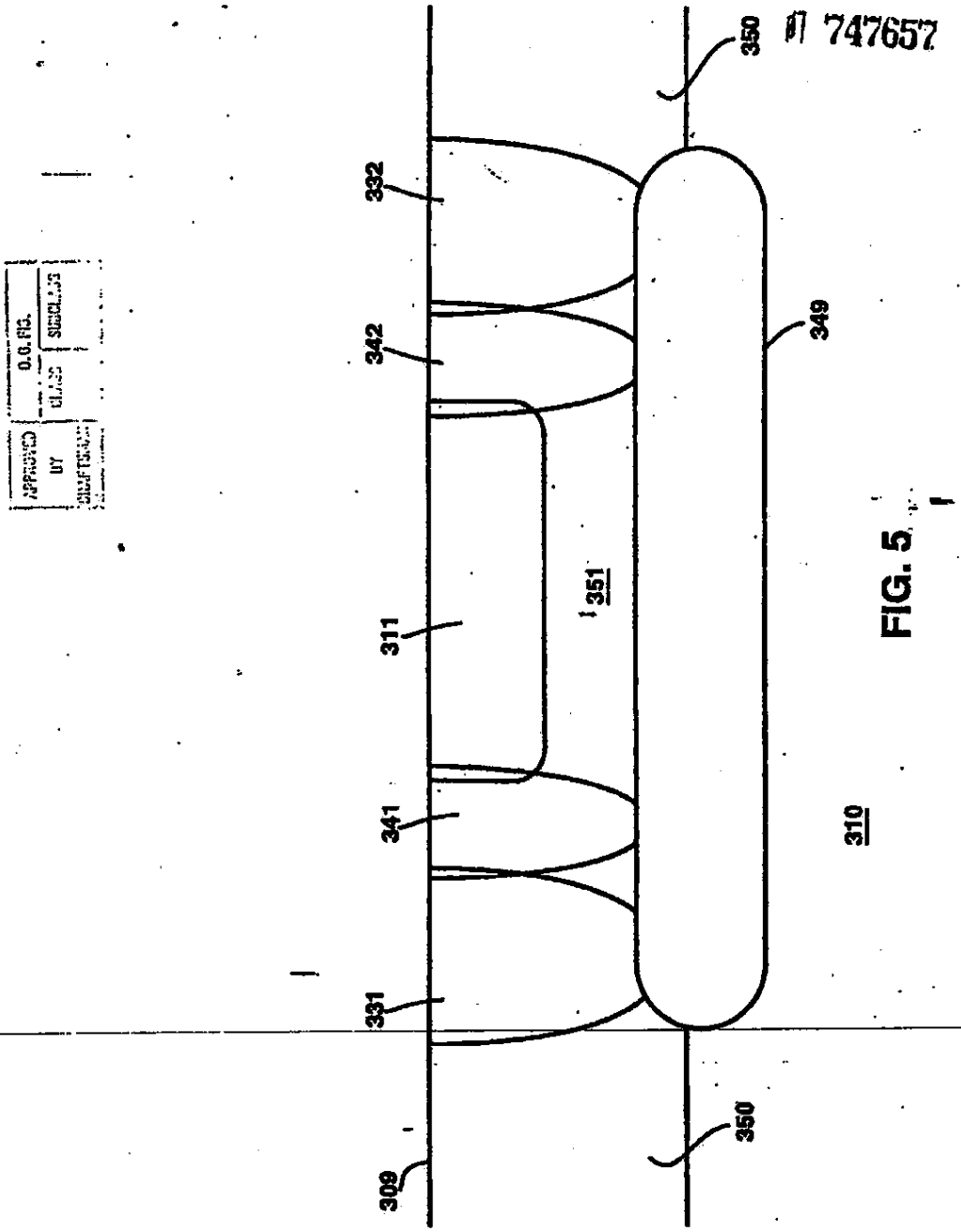

FIG. 5

DX 600

Optimum Design of Power MOSFETS

P.L.Hower, T.M.S.Heng and C. Huang

Unitrode Corporation
Watertown, Mass. 02172

ABSTRACT

Three cell geometeries (rectangle, square and hexagon) have been investigated using a lumped R_{ds} model. It is demonstrated that for each geometry one can calculate a spacing of the p-well diffusions that minimizes R_{ds}. This optimum spacing is a function of the vertical and lateral p-well dimensions, the desired breakdown voltage, and, in some cases, the average current density in the cell.

It is shown that in choosing the minimum R_{ds} for the typical range of breakdown voltages (50-1000V) and realizable cell sizes (20 to 40 μm), the square gives a smaller R_{ds} than the rectangle, and the hexagon gives a smaller resistance than the square. Therefore, the hexagon is the preferred geometry for these situations.

INTRODUCTION

At present there is some controversy as to the choice of cell geometries which minimize the on-resistance R_{ds} of power MOSFETS which are made using the vertical DMOS structure. To attack this problem it is necessary to have accurate models of current flow in the on-state. Previous authors (1,2) have used two-dimensional numerical solutions of the semiconductor differential equations to calculate on-resistance. This method will give accurate results for "long" rectangular or interdigitated cells, however, it is necessary to take into account three-dimensional current flow for other cell geometries. These alternate geometries are important because they give further reductions in R_{ds}.

The need for three-dimensional solutions greatly increases the computer memory requirements for numerical modeling. A further problem with numerical solutions is that computation time can become excessive when searching for the combination of cell parameters that minimizes R_{ds}.

For these reasons we have developed a lumped approximation to the components of on-resistance. Experimental checks of the model show that it accurately predicts R_{ds} for the range of cell parameters and drain region concentration and thickness combinations of interest.

ON-STATE MODEL

A number of authors have considered the problem of calculating the on-resistance of power MOSFETS (1-4), however, there has been no satisfactory analytical solution to the problem of determining current flow in the "neck" region between the p-wells. This problem is illustrated in Fig. 1 where

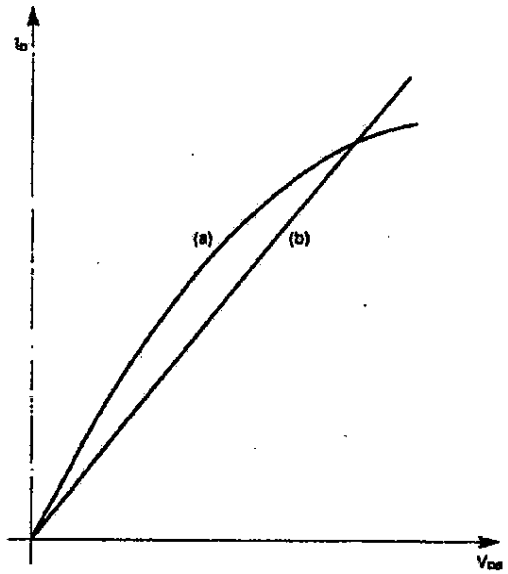

Fig.1. Drain characteristic showing a design (a) where R_{JFET} dominates the neck region and a design (b) with wider-spaced p-wells where the transfer resistance is dominant.

CH1973-7/83/0000-0087 $1.00 © 1983 IEEE

the I_D, V_{DS} characteristic is shown for two situations. In case (a), the distance ℓ_c between the p-wells is small and JFET action, (where the p-well diffusions act as gates of an n-channel JFET) causes the on-resistance to increase as I_D is increased. In case (b), ℓ_c is too large for JFET action to occur and current flow assumes a pattern which depends on the local geometry, the resistivity of the neck region, and the sheet resistance of the accumulation layer under the gate.

Neck Region Resistance

Cell cross-sections corresponding to the two cases of Fig. 1 are shown in Fig. 2, where

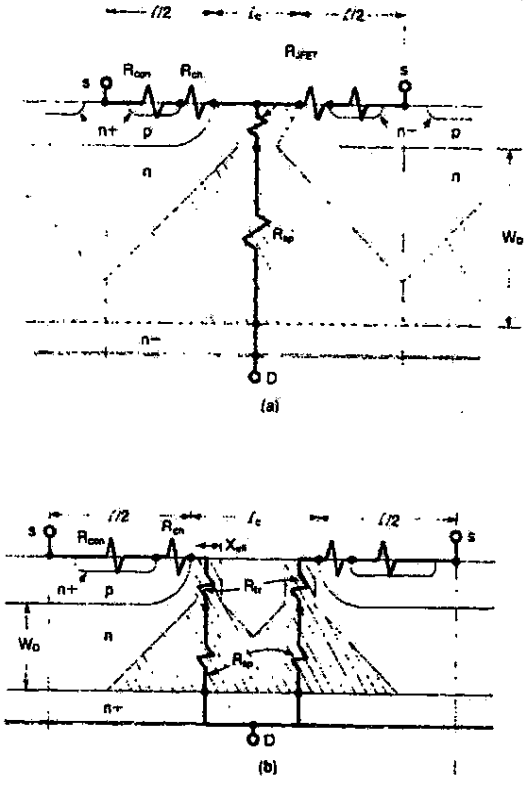

Fig.2. Two cases corresponding to the I-V characteristics of Figure 1. JFET action is dominant in (a) and current crowding due to the transfer of current flow from the accummulation layer is dominant in (b).

the center-lines indicate the extent of each unit cell. In Fig.2 (a) JFET action dominates. For this case the gradual channel solution is used to estimate R_{JFET} where the gate length is approximated by x_J, the p-well diffusion depth. The channel width near the pseudo-drain of this JFET determines the effective contact dimension of the drain spreading resistance R_{sp}.

Current flow in the n-layer is indicated in Figs.2 (a) and (b) by the shaded regions. A current flow spreading angle of 45 degrees (4) is used for a three-dimensional calculation of R_{sp}.

For large ℓ_c, R_{JFET} decreases and vertical current flow can no longer be taken as uniform over the source end of the neck region JFET. Upon entering the n-region from the inversion layer, current will transfer from a horizontal direction in the accumulation layer to a vertical direction in the n-layer.

To approximate this situation we have adapted the "transmission line model" which has been used to solve the problem of two-dimensional current flow at ohmic contacts, (5), (6). From this solution it can be shown that the vertical component of current flow exhibits a cosh-like distribution with respect to the center of the neck region. We approximate the situation as shown in Fig.2 (b), where an equivalent value of uniform current flow occurs over a distance x_{eff} which is given by

$$x_{eff} = \frac{L_T}{\tanh(\ell_c/2L_T)} \qquad (1)$$

L_T is the transfer length and is given by

$$L_T = \sqrt{\rho_D x_J/(3R_{sn+})} \qquad (2)$$

where ρ_D is the resistivity of the drain region and R_{sn+} is the sheet resistance of the accumulation layer.

Depending on the various cell parameters, either case (a) or (b) is used to find the neck region voltage drop. Other components of on-resistance which are accounted for in the analysis are the channel resistance R_{ch} and contact resistance to the n+ source region R_{con}.

Comparison with Experiment

The model for R_{DS} has been checked against experiment by considering both high and low voltage designs and wide and narrow neck regions. An example where R_{JFET} is dominant is shown in Fig. 3.

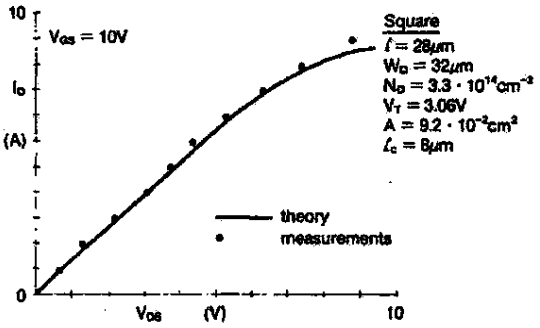

Fig.3. Measured and calculated drain characteristic for a high voltage design (BV = 430V) where R_{JFET} dominates.

In another example, which is a lower voltage design, R_{tr} is dominant. Measurements are compared against theory for this example in Fig.4,

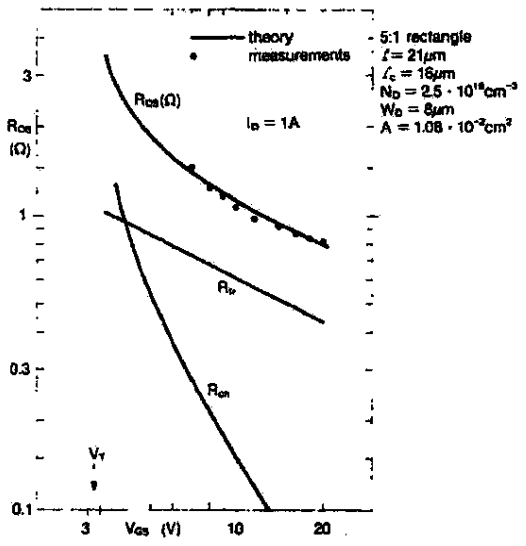

Fig. 4. Measured and calculated R_{ds} vs. V_{GS} at I_D = 1A for a low voltage design (BV = 130V) where R_{tr} dominates.

where R_{DS} is now independent of I_D and is plotted vs. V_{GS} to show the influence of the accumulation layer. It can be seen in both cases that the model shows good agreement with measured values.

DESIGN CONSIDERATIONS

Optimum p-well Spacing

If we consider the case where the lateral p-well dimension ℓ is fixed we can determine an optimum spacing ℓ_{co} for the p-wells. This idea is not new, however, by improving upon the model of Ref.7 the present analysis permits a more accurate determination of ℓ_{co}. Therefore, the minimum on-resistance is also known with more accuracy. Fig.5 shows

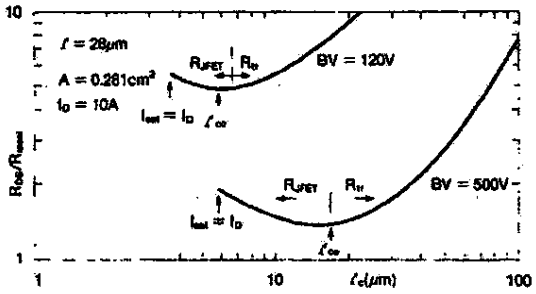

Fig.5. Normalized R_{DS} vs. p-well spacing for two different breakdown voltages. The optimum solution is indicated.

a plot of R_{DS}/R_{ideal} vs. ℓ_c for two examples. R_{ideal} is the resistance obtained for the drain region, assuming the entire cell area is conducting uniformly.

Comparison of Geometries

Fig. 6 shows plots of the product of on-resistance and "active" area A vs. breakdown voltage. The active area is the portion of the die that is available for cells. For these plots the drain doping and thickness are adjusted to give the minimum R_{DS} for each BV, assuming uniform current flow. The source window dimension ℓ is fixed at 30 μm which is consistent with conventional photolithographic limits (minimum feature size in the 5 to 6 μm range). For each BV, ℓ_c is adjusted to give the minimum R_{DS}.

Fig. 6 is a demonstration of the earlier claim that for the three geometries considered, the hexagon will give the minimum on-resistance.

These results are consistent with the previous observation that R_{DS} deviates considerably from R_{ideal} as BV is reduced (8). The present analysis shows that less efficient spreading of the current in the drain region and the increased importance of the transfer resistance account for most of the deviation at the lower values of BV.

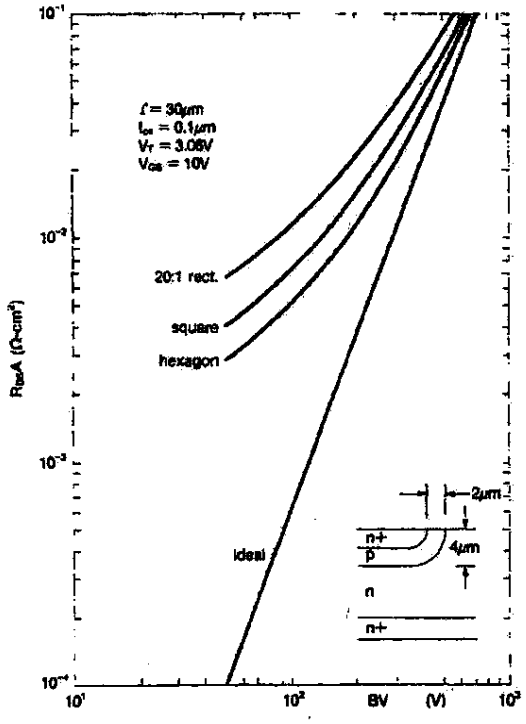

Fig. 6. Specific on-resistance vs. breakdown voltage for different geometries.

By calculating minimum R_{DS}(on) for different size p-wells we can see how improvements in processing and photolithography will decrease R_{DS}. A comparison between the square and the hexagon is carried out in Fig. 7 and 8 where R_{DS}/R_{ideal} is plotted vs. p-well size for a high and low breakdown voltage design. Note the difference in vertical scales.

It can be seen from these two figures that only minor improvements can be made in high voltage MOSFETs by shrinking geometries, however, the on-resistance for low-voltage designs can be decreased by about a factor of two if ℓ is decreased from 30 to 8 μm.

In conclusion we have found that the analysis described in this paper is a useful design tool. It also permits an identification of possible trends for future design of power MOSFETs.

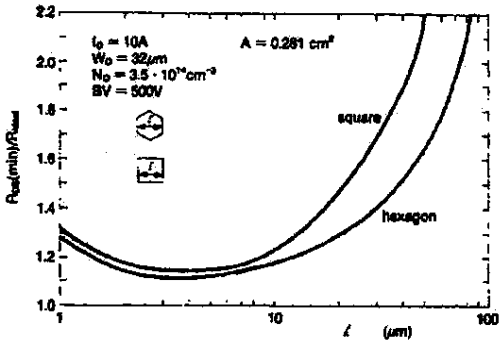

Fig.7. Normalized optimum R_{DS} vs. p-well size for hexagonal and square geometries, BV = 500V.

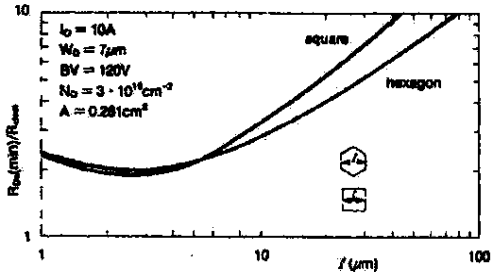

Fig.8. Similar to Figure 7 but for BV = 120V.

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2. A. Nakagawa, et al, "High Voltage Low-On-resistance VDMOS FET,"Japanese Journal of Applied Physics,V.21 (1982) supplement 21-1 pp.97-101.
3. S.C.Sun and J.D.Plummer,"Modeling of the on-resistance of LDMOS,VDMOS, and VMOS Power Transistors,"IEEE Trans. on Elec.Dev.,V.ED-27, pp.356-367, Feb.1980.
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8. R.P.Love,P.V.Gray, & M.S.Adler,"A Large Area Power MOSFET Designed for Low Conduction Losses" 1981 IEDM Digest, pp. 418-421.

DX 601

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/008,324	11/09/2006	6107851	10414-25	6695

7590 12/19/2006

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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 12/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Case No. 04-1371-JJF
DEFT Exhibit No. DX 601
Date Entered _____
Signature _____

PTO-90C (Rev. 10/03)

Order Granting / Denying Request For Ex Parte Reexamination	Control No.	Patent Under Reexamination	
	90/008,324	6107851	
	Examiner	Art Unit	
	Margaret Rubin	3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed *09 November 2006* has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☒ PTO/SB/08, c)☐ Other: _____

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

a) ☐ by Treasury check or,

b) ☐ by credit to Deposit Account No. _____, or

c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).

Margaret Rubin
Primary Examiner
Art Unit: 3992

cc:Requester (if third party requester)

DECISION GRANTING *EX PARTE* REEXAMINATION

Information Submissions

Information Submissions in *Ex Parte* Proceedings are bound by 37 CFR § 1.555 which incorporates 37 CFR § 1.98(a). Establishing a publication date for non-patent literature is among the requirements of 37 CFR § 1.98(a). Insofar as Requester has not provided the same for citation CE, this reference has not been considered and has been lined through on the information disclosure statement. Furthermore, it appears as if Requester made a typographical error in transcribing the title of citation CB and page numbers were not supplied for citations CC and CD. Corrections have been made by the Office on PTO form 1449.

Summary

Substantial new questions of patentability affecting claims 1, 2, 4, 7, 9, 10, 11, 13, 16 and 17 of United States Patent No.

6,107,851 (hereafter "the base patent") are raised by the following references[1]:

[1] An SNQ is not raised by LM3101 Secondary-Side PWM Controller; National Semiconductor, cite "CE" of the IDS, because Requester has not established that a publication date for the document. Thus, whether it qualifies as prior art under 35 USC 102 is unknown.

1.) SGS-Thomson TEA 2262 Datasheet, "Switch Mode Power Supply Controller", pp 1-9, (April 1996) (hereafter, "TEA 2262");

2.) SGS-Thomson TEA 2260/TEA2261, Datasheet Application Note 376, "High Performance Driver Circuits for S.M.P.S." pp. 1-33 (June 1994) (hereafter, "TEA 2260/2261");

3.) PWM Power Supply IC; 85-265 VAC Input Isolated, Regulated DC Output, Power Integrations SMP211 Datasheet (January 1996) (hereafter, "SMP 211");

4.) U.S. Patent No. 4,638,417 to Martin;

5.) "Programmed Pulsewidth Modulated Waveforms for Electromagnetic Interference Mitigation in DC-DC Converters"; IEEE Transactions on Power Electronics, Vol. 8, No.4 (October 1993) by A.C. Wang and S.R. Sanders, pp. 596-605 (hereafter "Wang");

6.) U.S. Patent No. 5,498,995 to Szepesi et al., (hereafter "Szepesi); and

7.) "Off-Line Power Integrated Circuit for International Rated 60-watt Power Supplies" by Richard Keller, Applied Power Electronics Conference and Exposition, February 1992 (pp. 505-512) (hereafter, "Keller").

Issues Raised by Requester

Although the merits of the rejections suggested in the request are not decided herein, it is noted that the Requester proposes that the references supplied raise substantial new questions of patentability when viewed in the following manner:

1.) Claims 1, 2, 4, 7, 9, 10, 11, 13, 16 and 17 are rejected under 35 U.S.C. §§102(a)(b) as anticipated by TEA 2262;

2.) Claims 1, 2, 4, 7, 9, 10, 11, 13, 16, and 17 are rejected under 35 U.S.C. §§102(a)(b) as anticipated by SMP211 in light of the admitted prior art of the patent;

3.) Claims 1, 2, 7, 9, 10, 11, 16, and 17 are rejected under 35 U.S.C. §§102(a)(b) as anticipated by Martin;

4.) Claims 1, 2, 7, 9, 10, 11, 16, and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Martin in view of SMP211;

5.) Claims 4 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Martin in view of Keller;

6.) Claims 1, 2, 7, 9, 10, 11, 16, and 17 are rejected under 35 U.S.C. §§102(a)(b) as anticipated by Wang;

7.) Claims 4 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Wang in view of Keller; and

8.) Claims 1, 2, 7, 9, 10, 11, 16, and 17 are rejected under 35 U.S.C. §§102(a)(b) as anticipated by Szepesi.

Background

The base patent issued from United States Patent Application No. 09/080,774 (hereafter "the base application"). Although Office records of the prosecution history of the base application are not currently available and will not be available in a timely manner for purposes of deciding this request, insofar as Requester has provided papers from the prosecution history, they have been reviewed to determine what claim limitations were deemed patentable. It is noted that a statement regarding allowable subject matter dated December 13, 1999 cited "a PWM switch comprising an oscilator [*sic*] for generating a maximum duty cycle signal and a singnal [*sic*] with a frequency range dependent on a frequency variation circuit as recited in claim 1." It is noted that there are two independent claims within the base patent: claims 1 and 11. Neither of them include recitation of a signal with a frequency range dependent on a frequency variation circuit. In addition, claim 11 does not

require a PWM switch. Lastly, from the records supplied by Requester, it appears as if a Statement of Reasons for Allowance was not made when the base application was allowed.

In summary, the prosecution history does not provide a clear record of the reasons the base patent was allowed.

Issues

TEA 2262 and TEA 2260/2261

It is agreed that TEA 2262 and TEA 2260/2261 raise an SNQ for claims 1 and 11. Insofar as Requester has grouped these references together for presentation, they have been evaluated together herein. (That said, these references could not fairly be treated as a single publication for purposes of making a rejection under 35 USC 102 as suggested by Requester.) More particularly, Requester has provided plausible item-matching for a number of limitations of claims 1 and 11 on pages 10-15 and 20-26, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings presented in the request cannot be judged as merely cumulative. By raising an SNQ with regard to the independent claims, an SNQ is also raised

for the dependent claims 2, 4, 7, 9, 10, 13, 16 and 17 which come freighted with the limitations of the claims from which they stem.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

SMP211

It is agreed that SMP 211 raises an SNQ for claims 1 and 11. More particularly, Requester has provided plausible item-matching for a number of limitations of claims 1 and 11 on pages 31-34 and 39-42, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings presented in the request cannot be judged as merely cumulative. By raising an SNQ with regard to the independent claims, an SNQ is also raised for claims 2, 4, 7, 9, 10, 11, 13, 16 and 17 which come freighted with the limitations of the claims from which they stem.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Martin

It is agreed that Martin raises an SNQ for claims 1 and 11. More particularly, Requester has provided plausible item-matching for a number of limitations of claims 1 and 11 on pages 46-49 and 55-59, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings presented in the request cannot be judged as merely cumulative. By raising an SNQ with regard to the independent claims, an SNQ is also raised for claims 2, 4, 7, 9, 10, 13, 16 and 17 which come freighted with the limitations of the claims from which they stem.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination

and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Keller

It is agreed that Keller raises an SNQ for claims 4 and 13. More particularly, Requester has provided plausible item-matching for a number of limitations of claims 4 and 13 at least on pages 50-51 and 59-60, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings presented in the request cannot be judged as merely cumulative.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Wang

It is agreed that Wang raises an SNQ for claims 1 and 11. More particularly, Requester has provided plausible item-

matching for a number of limitations of claims 1 and 11 on pages 67-70 and 75-79, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings presented in the request cannot be judged as merely cumulative. By raising an SNQ with regard to the independent claims, an SNQ is also raised for claims 2, 4, 7, 9, 10, 11, 13, 16 and 17 which come freighted with the limitations of the claims from which they stem.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Szepesi

It is agreed that Szepesi raises an SNQ for claims 1 and 11. More particularly, Requester has provided plausible item-matching for a number of limitations of claims 1 and 11 on pages 84-89 and 94-100, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings

presented in the request cannot be judged as merely cumulative. By raising an SNQ with regard to the independent claims, an SNQ is also raised for claims 2, 4, 7, 9, 10, 11, 13, 16 and 17 which come freighted with the limitations of the claims from which they stem.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Conclusion

Since Requester did not request reexamination of claims 3, 5, 6, 8, 12, 14, 15 and 18 and did not assert the existence of a substantial new question of patentability (SNQ) for such claims, these claims will not be reexamined unless at the discretion of the Office.

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires

that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No 6,107,851 throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

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Margaret Rubin
Primary Examiner
Central Reexamination Unit 3992
(571) 272-1756

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if Known	
Patent Number	6,107,851
Issue Date	June 19, 2001
First Named Inventor	Balu Balakirshnan
Group Art Unit	3992
Examiner Name	Rubin
Attorney Docket Number	

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	U.S. Patent Document Number	Kind Code[2]	Name of Patentee or Applicant of Cited Document	Date of Patent of Cited Documents MM-DD-YYYY
MR	AA	4,638,417		Hubert C. Martin, Jr. ,et al.	January 20, 1987
MR	AB	5,498,995		Thomas Szepesi	March 12, 1996

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5]	Name of Patentee or Applicant of Cited Document	Date of Publications of Cited Documents MM-DD-YYYY	T[6]
	BA						

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
MR	CA	SGS-Thomson Microelectronics TEA 2262; Switch Mode Power Supply Controller; pages 1-9; April 1996	
MR	CB	SGS-Thomson Microelecronics TEA ~~2262~~ 2260/TEA2261; High Performance Driver Circuits for S.M.P.S; pages 1-33; June 1994	
MR	CC	PWM Power Supply IC; 85-265 VAC Input Isolated, Regulated DC Output; Power Integrations SMP211 Datasheet (January 1996) ("SMP 211") pp 2-4 to 2-5 and pp 5-1 to 5-6	
MR	CD	"Programmed Pulsewidth Modulated Waveforms for Electromagnetic Interference Mitigation in DC-DC Converters; IEEE Transactions on Power Electronics, Vol. 8, No. 4 (Oct 1993) A.C. Wang, S.R. Sanders pp 596-605	
	CE	~~LM3101 Secondary-Side PWM Controller, National Semiconductor, Szepesi~~	
MR	CF	Off-Line Power Integrated Circuit For International Rated 60 Watt Power Supplies; Richard Keller, Power Integrations Inc. Page 505-512, IEEE 1992	

Examiner Signature	OHS West:260122431.1	Date Considered	12/8/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent documents. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

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DX 602

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/008,327	11/09/2006	6229366	10414-25	7730

7590 01/22/2007

EXAMINER

James Y. Go
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
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Los Angeles, CA 90025-1026

ART UNIT	PAPER NUMBER

DATE MAILED: 01/22/2007

Please find below and/or attached an Office communication concerning this application or proceeding.

Case No. 04-1371-JJF
DEFT Exhibit No. DX 602
Date Entered _____
Signature _____

PTO-90C (Rev. 10/03)

Order Granting / Denying Request For Ex Parte Reexamination	Control No.	Patent Under Reexamination	
	90/008,327	6229366	
	Examiner	Art Unit	
	Margaret Rubin	3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed *09 November 2006* has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☒ PTO/SB/08, c)☐ Other: _____

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

a) ☐ by Treasury check or,

b) ☐ by credit to Deposit Account No. _____, or

c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).

Margaret Rubin
Primary Examiner
Art Unit: 3992

cc:Requester (if third party requester)

DECISION GRANTING *EX PARTE* REEXAMINATION

Information Submissions

Information Submissions in *Ex Parte* Proceedings are bound by 37 CFR § 1.555 which incorporates 37 CFR § 1.98(a). It appears as if Requester made typographical errors in transcribing the title of citation CB and the date of citation CC. Further, page numbers were not supplied for citations CB, CC and CD. Corrections have been made by the Office on PTO form 1449.

Summary

Substantial new questions of patentability affecting claims 1, 2, 8, 9, 10, 14, 16 and 18 of United States Patent No. 6,229,366 (hereafter "the base patent") are raised by the following references:

1.) SGS-Thomson "TEA2262, Switch Mode Power Supply Controller" pp. 1-9 (April 1996) (hereafter, "TEA2262");

2.) U.S. Patent No. 4,638,417 to Martin;

3.) "Programmed Pulsewidth Modulated Waveforms for Electromagnetic Interference Mitigation in DC-DC Converters"; IEEE Transactions on Power Electronics, Vol. 8, No.4 (October 1993) by A.C. Wang and S.R. Sanders, pp. 596-605 (hereafter "Wang");

4.) Unitrode UCC 3800/1/2/3/4/5 biCMOS Current Mode Control IC's, Bill Andreycak, pp. 9-344 - 9-361 (1994) ("U-133") and

5.) "Off-Line Power Integrated Circuit for International Rated 60-watt Power Supplies" by Richard Keller, Applied Power Electronics Conference and Exposition, February 1992 (pp. 505-512) (hereafter, "Keller").

Issues Raised by Requester

Although the merits of the rejections suggested in the request are not decided herein, it is noted that the Requester proposes that the references supplied raise substantial new questions of patentability when viewed in the following manner:

1.) "Claims 1, 2, 8, 9, 10, 14, 16 and 18 are rejected under 35 U.S.C. §§102(a)(b) as anticipated by TEA2262";

2.) "Claims 1, 2, 8, 9, 10, 16 and 18 are rejected under 35 U.S.C. §§102(a)(b) as anticipated by Keller";

3.) "Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Keller in view of Martin or, alternatively, in view of Wang"; and

4.) "Claims 1, 2, 8, 9, 10, 16, and 18 are rejected under 35 U.S.C. §§102(a)(b) as being anticipated U-133."

Background

The base patent issued from United States Patent Application No. 09/573,081 (hereafter "the base application").

The base application was allowed in the first Office action. It is noted that a statement regarding allowable subject matter mailed December 13, 2000 cited "a pulse width modulation circuit comprising a switching transistor wherein the switching transistor can be driven into a non-conducting state by a maximum duty cycle signal, a drive circuit, or a soft start circuit." It is noted that there are two independent claims within the base patent: claims 1 and 9. Neither of them include recitation of a switching transistor. In addition, claim 9 does not require a pulse width modulation circuit, or a maximum duty cycle signal. Lastly, claim 1, for instance, requires that a switch allows a signal to be transmitted between first or second terminals in accordance with a drive signal. The drive signal is provided "according to said maximum duty cycle signal" and a signal from the soft start circuit instructs the drive circuit "to disable said drive signal during at least a portion of said on-state of said maximum duty cycle." Assuming that the switch recited in claim 1 correlates with the switching transistor of the before mentioned reasons for allowance, the reasons for allowance describes different causal relationships between recited elements. In a similar fashion, the causal relationship between recited elements of claim 9 differs from the description included in the reasons for allowance.

In summary, the prosecution history does not provide a clear record of the reasons the base patent was allowed.

TEA 2262

It is agreed that TEA 2262 raises an SNQ for claims 1 and 9. More particularly, Requester has provided plausible item-matching for a number of limitations of claims 1 and 9 on pages 8-12 and 15-18, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings presented in the request cannot be judged as merely cumulative. By raising an SNQ with regard to independent claims 1 and 9, an SNQ is also raised for the dependent claims 2, 8, 10, 14, 16 and 18 which come freighted with the limitations of the claims from which they stem.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Keller

It is agreed that Keller raises an SNQ for claims 1 and 9. More particularly, Requester has provided plausible item-matching for a number of limitations of claims 1 and 9 on pages 24-25 and 29-31, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings presented in the request cannot be judged as merely cumulative. By raising an SNQ with regard to independent claims 1 and 9, an SNQ is also raised for the dependent claims 2, 8, 10, 16 and 18 which come freighted with the limitations of the claims from which they stem.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Martin and Wang

It is agreed that Martin and Wang raise an SNQ for claim 14. More particularly, Requester has provided plausible item-

matching for a number of limitations of claim 14 on pages 32-35, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings presented in the request cannot be judged as merely cumulative.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

U-133

It is agreed that U-133 raises an SNQ for claims 1 and 9. More particularly, Requester has provided plausible item-matching for a number of limitations of claims 1 and 9 on pages 41-42 and 44-45, respectively, of the request. In view of the fact that the prosecution history does not provide a clear record of the reasons the base patent was allowed, the teachings presented in the request cannot be judged as merely cumulative. By raising an SNQ with regard to independent claims 1 and 9, an SNQ is also raised for the dependent claims 2, 8, 10, 16, and 18

which come freighted with the limitations of the claims from which they stem.

Such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Conclusion

Since Requester did not request reexamination of claims 3-7, 11-13, 15 and 17 and did not assert the existence of a substantial new question of patentability (SNQ) for such claims, these claims will not be reexamined unless at the discretion of the Office.

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in

ex parte reexamination proceedings are provided for in 37 CFR 1.550(c).

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No 6,229,366 throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

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/M Rubin/

Margaret Rubin
Primary Examiner
Central Reexamination Unit 3992
(571) 272-1756

conferees:

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known 11/09/06	
Patent Number	6,229,366
Issue Date	May 8, 2001
First Named Inventor	Balu Balakirshnan
Group Art Unit	3992
Examiner Name	Rubin
Attorney Docket Number	

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	U.S. Patent Document Number	Kind Code[2]	Name of Patentee or Applicant of Cited Document	Date of Patent of Cited Documents MM-DD-YYYY
MR	AA	4,638,417		Hubert C. Martin, Jr.	01/20/1987
	AB				

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5]	Name of Patentee or Applicant of Cited Document	Date of Publications of Cited Documents MM-DD-YYYY	T[6]
	BA						

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

...aminer Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
MR	CA	SGS-Thompson datasheet entitled "TEA2262, Switch Mode Power supply Controller," pp. 1-9 (April 1996) ("TEA2262").	
MR	CB	R. Keller, "~~Power Integrations~~," Off-Line Power Integrated Circuit for International Rated 60-Watt Power Supplies," (February 23-27, 1992) Keller pp 505 - 512	
MR	CC	"Programmed Pulsewidth Modulated Waveforms For Electronagetic Interferences Mitigation In DC-DC Converters", IEEE Transactions on Power Electronics, Vol. 8, No. 4 (October ~~1993~~) A.C. Wang and S.R. Sanders ("Wang"). pp 596 - 605 1993	
MR	CD	Unitrode UCC 3800/1/2/3/4/5 biCMOS Current Mode Control IC's (1994) ("U-133") pp 9-344 - 9-361	

Bill Andreycak

...aminer gnature	M Rubin	Date Considered	1/3/07

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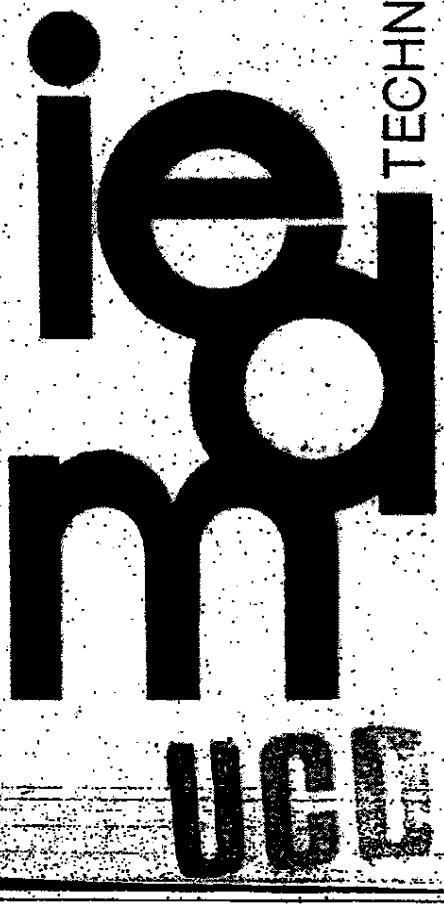

Late News!
Page 819

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MONOLITHIC MOS HIGH VOLTAGE INTEGRATED CIRCUITS

James D. Plummer

Integrated Circuits Laboratory
Stanford University

ABSTRACT

Two general classes of high voltage MOS IC's may be defined. The first is structured around a conventional NMOS or PMOS technology and adds ion implanted extended drain regions, offset or stacked gates, or lightly doped drain regions to produce high voltage (50-300 volt) output devices. Such devices are generally operated with a grounded source, have an enclosed geometry, are relatively high on-resistance, and have found some application primarily in display driving. A second, more flexible technology is structured around lateral DMOS devices similar to the discrete power FET devices now widely available commercially. This technology generally uses N⁻ epitaxial layers on P⁺ substrates, junction isolation, and is compatible with high voltage PMOS and N channel DMOS devices, and low voltage logic devices. This paper will primarily address the latter class of circuits and will consider practical problems of high voltage device design, power dissipation limitations, parasitic surface and bulk devices, and approaches to level shifting low level logic inputs to high voltages.

INTRODUCTION

Discrete high voltage power MOS devices based upon double-diffused DMOS structures have recently received substantial commercial and research interest. Integration of high voltage MOS devices in monolithic circuits has proceeded at a much slower pace although substantial applications in display driving, power control, telephony, and other areas exist. This paper will discuss the device and technology problems which arise in functional integration of high voltage MOS devices alongside low voltage logic or signal processing devices, and present approaches to their solution along with experimentally fabricated examples.

Two general classes of high voltage MOS integrated circuits exist. The first is structured around a conventional NMOS or PMOS technology and by minor modifications to these processes produces output devices with voltage capabilities of 50-300+ volts. These output devices use ion implanted extended drain regions, offset or stacked gates, or lightly doped drain regions to achieve high voltage operation. An example of such a structure is shown schematically in Fig. 1, based in this case on a conventional NMOS silicon gate technology.

In this example, a lightly doped ion implanted N⁻ drift region is placed between the active device channel and the N⁺ drain contact. The gate electrode extends over this N⁻ region on top of thick oxide, helping to shape the surface fields in the structure, thus acting as a field plate. Such devices depend for their high voltage capability on the N⁻ region supporting most of the applied voltage. A number of examples of this approach have appeared in the literature [1,2], based upon either NMOS or double-diffusion (DMOS) devices as the active switching element. Conceptually similar approaches, based upon thin N⁻ epitaxial layers have also recently been proposed [3,4]. These latter structures have been named Resurf devices after the manner in which electric fields are controlled; they operate, however, in a similar fashion to the device illustrated in Fig. 1. Operation of all of these devices at the highest voltage levels implies that the N⁻ region under the extended gate electrode must be completely depleted in the off state. This shifts the region of highest electric field away from the surface and into the bulk. Several empirical and computer simulated studies of the optimum N⁻ implant dose in these devices [1,3], have independently arrived at doses of $0.5\text{-}2\times10^{12}/cm^2$, reflecting the need for complete N⁻ depletion if the highest possible voltages are to be achieved.

Such devices generally operate in a grounded source configuration because they are inherently assymetric in their voltage capability. They also generally utilize an enclosed geometry with the drain bonding pad in the center in order to avoid parasitic field inversion problems. As a consequence of the lightly doped N⁻ region, these devices are generally fairly high on-resistance structures. This type of technology has been used primarily for display driving applications in which the grounded source and relatively low current capability of the output devices are acceptable. The basic NMOS or DMOS process used to build the devices makes it straightforward to implement complex logic functions on the same chip with the high voltage output devices. Alternative approaches to high voltage output devices have utilized offset [5] or stacked [6] gate electrodes with generally the same limitations on grounded source, low current applications.

A second general type of high voltage MOS integrated circuit is based upon DMOS technology [7]. Such devices are generally fabricated in thick N⁻ epitaxial layers on P⁺ substrates and use junction isolation. Lateral DMOS devices are employed because they provide access to all three

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device terminals on the top wafer surface for easy interconnect to other devices. The combination of a short active channel and a lightly doped drift region provides high voltage, high speed and low on-resistance in the DMOS device. Such devices are directly compatible with low voltage PMOS devices to implement logic functions, as illustrated schematically in Fig 2. Low voltage N channel DMOS devices may also be used to implement CMOS logic; this, however, is not area efficient because each of the DMOS devices requires its own isolation region. The remainder of this paper will concentrate on this second type of circuit. The use of thick epitaxial layers removes the restriction of grounded source operation and thus makes possible a wider range of applications.

An example of an integrated circuit fabricated with the technology of Fig. 2 is shown in Fig. 3. The large area devices are high voltage (125 volt), high current (0.3 Amp), low on resistance (<50Ω) analog switches, implemented with DMOS devices. The central portion of the chip contains PMOS logic for selecting 1 out of 8 of the analog switches and level shifting circuits to control the on or off state of the high voltage channels. Each of the analog channels can be selected in <3 μsec and can switch analog or digital signals up to 10 MHz and 125 volts. The overall chip size is 4 × 4 mm. Higher voltage versions of this chip have been implemented, to switch analog signals up to 175 volts.

COMPATIBLE LOGIC DEVICES

Any generally useful high voltage technology must be capable of implementing high performance, low voltage logic functions. This is necessary both for interfacing with other circuits and because it is very costly in terms of power and chip area to utilize high voltage devices where they are not needed. The technology illustrated in Figures 2 and 3 uses conventional PMOS devices for low voltage logic. This is attractive because all of the logic can be placed in a single isolated N^- region. Vertical NPN and lateral PNP bipolar transistors are also compatible with the basic eight mask process as are N channel DMOS devices. These latter three, however, have the major disadvantage of requiring isolated N^- regions. This is a substantial penalty in high voltage circuits because thick epitaxial layers (≈25-30μ for 200 volt operation) imply large N^- regions to allow for lateral diffusion of the P^+ isolation and to support large voltages between the substrate and the epi layer. Dielectric isolation techniques would clearly circumvent some of these problems.

Additional processing steps can be used to implement conventional NMOS devices. Specifically, the addition of an ion implanted P well in an isolated N^- region and any threshold shifting implants required, have been used to fabricate high performance NMOS logic [8]. Such a process, however, is substantially more complicated than the basic technology of Fig. 2, often requiring more than 11 masking steps and several critical ion implants.

It is well known that high voltage DMOS devices can be fabricated in P type regions. This would suggest the possibility of fabricating high voltage MOS circuits in P type epitaxial layers on N type substrates. Such a process would be directly compatible with high performance NMOS logic, although this type of structure has not been reported.

LEVEL SHIFTING CIRCUITS

Most high voltage integrated circuits must at some point accomplish a level translation between low voltage logic levels and the high voltages which are to be controlled. In circuits of the type shown in Fig. 1, this process is straightforward because standard logic levels can drive the gate of the high voltage output device directly. In the more general case, such as the type of circuit illustrated in Figures 2 and 3, a function of the type shown in Fig. 4 must be implemented. Such a circuit is a key element in many high voltage designs. The circuit shown in Fig. 4 is meant to be only a conceptual realization. Practical implementations will be described later.

It is important to note that the level shifting function cannot be realized without significant amounts of DC power dissipation, particularly when high speed switching is required, unless dynamic circuits are used. CMOS approaches do not solve this problem because the input signals do not approach the 1V levels and therefore cannot switch the active devices completely off. A simple calculation illustrates this point.

If the voltage levels are ±100 volts, the required switching time is 1 μsec and the load on each stage is ≈ 1pf (this is not unusual in large geometry high voltage devices), then the current sources I_1, and I_2 must supply 100 and 200μA respectively. This implies an average DC power dissipation of ≈ 25mw assuming a 50% duty cycle. Clearly large numbers of such circuits cannot be integrated on a single chip with reasonable power limits. It should also be noted however, that both stages in the circuit of Fig. 4 consume power when the logic input is high. Level shifting first to the negative supply and then to the positive supply would reverse this. As a result, knowledge of expected system logic states can be used to adapt level shift design and hence minimize power dissipation.

A specific example of a level translating circuit is shown in Fig. 5, along with a photomicrograph of a portion of an integrated circuit using this design. Two such circuits are shown in the photomicrograph. The high voltage PMOS device in the second stage uses two cascaded transistors to divide the applied voltage and thick oxide (1.5μ field oxide) gates, since high voltages are present to drive the gates. The unusual metal pattern in these devices is used to minimize parasitic field inversion effects and will be described later.

HIGH VOLTAGE ANALOG SWITCHES

Switching of high voltage analog or digital signals requires careful device design and attention to parasitic devices. Previous circuits designed to do this have made use of a single high voltage DMOS transistor operated as a transmission gate [7]. Such a device, as shown in Fig. 2, has

the distinct disadvantage of being assymetric because of the presence of a diode between source and drain. More recent work, as represented by the chip in Fig. 3, has made use of two DMOS devices in series, with the intrinsic diodes back to back.

This analog switch is shown schematically in cross-section in Fig. 6. The two gates are connected together as are the two source regions. A diode, fabricated alongside the switches is connected between the two source regions and the two gates as shown. In the off state, the gate is held at a voltage more negative than the signal being switched by, for example, a circuit of the type shown in Fig. 5. The diode pulls the two source regions to approximately this same potential. This allows either input/output terminal to assume any potential between -V and +V without the switch conducting. In the on state, the gate is biased to +V, turning on both DMOS devices and permitting analog or digital signals having any value between -V and $+V-V_{TH}$ to be passed. Voltage ratings up to ±100 volts and current capabilities of ±0.3 Amps are quite feasible with this type of switch as the chip in Fig. 3 illustrates. The geometric layout is quite similar to that reported earlier for a single high voltage DMOS device [7].

Several parasitic devices are present in the structure of Fig. 6. Most of these are common to all types of high voltage technologies. Surface inversion of the lightly doped N^- region is a concern which will be addressed later. In addition, vertical PNP and NPN transistors are present. One manifestation of these devices is illustrated in the analog switch I-V characteristics in Fig. 7. When the voltage across the switch exceeds ≈1.5 volts, a "kink" is observed in the characteristic. This has the beneficial effect of reducing the switch on-resistance at high current levels (in this case for I ≥ 30 mA).

The reason for this effect is the forward biasing of the P^+N^- bulk to drain diode in the DMOS device. If, for example, the right hand I/O terminal is at a positive voltage and the left hand side is at ground, then voltage drops greater than ≈0.7 volts across the left hand DMOS device will forward bias the P^+N^- diode. This diode is in parallel with the surface channel of the device; once the diode turns on its lower impedance bypasses the surface channel, resulting in an apparent reduction in overall device on-resistance. This effect does not occur when the device is switched off by the gate or when small signal currents are being carried because currents larger than 30mA are required to initiate forward biasing of the diode.

Two potential problems arise because of this effect. The first is the possibility of regenerative switching because of the presence of a four layer NPNP vertical device. This possibility can be easily minimized by effective shorting of the DMOS N^+ source and P channel regions as shown in the figure. The second problem is associated with the presence of vertical PNP transistors. Forward biasing of the P^+N^- diode results in hole injection into the N^- epi layer and subsequent collection of some of these holes by the P^- substrate. This implies that some fraction of the signal current will be shunted to the substrate. In applications in which this presents a problem, the use of N^+ buried layers or dielectric isolation techniques can minimize these parasitics.

Finally, it should be pointed out that parasitic bipolar transistors are always present in DMOS devices. In discrete power devices, they can result in reduced tolerance to high voltages and in thermal runaway problems. In integrated circuits these problems and additional ones associated with the specific circuit (such as those described above), must be considered in device and technology design.

SURFACE INVERSION PROBLEMS

Lightly doped regions which are necessary for high voltage operation are inherently subject to surface inversion. In a circuit of even modest complexity, the need to route metal lines around on the surface for device interconnect will nearly always result in some situations in which the voltages on the metal lines are large enough to invert the underlying surface. The classical approach to this problem has been to use guard rings as illustrated in Fig. 8. In the particular example illustrated here, the metal line has a potential of the correct polarity to invert the underlying N^- surface, and hence to cause conduction between the P^+ region on the left and the isolation region on the right. The N^+ region in the center will prevent this inversion.

The use of these guard rings can, however, significantly degrade device voltage capability. The high surface fields near the edges of the N^+ guard ring can cause avalanche breakdown at a voltage which is dependent on the oxide thickness and N^+ doping profile [9]. As a typical example, a 1.3μ oxide thickness and a 2μ deep, heavily doped N^+ region will break down at ≈130-150 volts [9]. This may be well below the voltage at which the circuit could otherwise operate.

One solution to this problem is to eliminate the N^+ guard rings and simply accept the leakage currents associated with these parasitic field oxide devices. The unusual metal layout in the PMOS devices in Fig. 5 is an example of this (the layout makes the effective length of the parasitic path long, thereby reducing the parasitic PMOS W/L ratio). A second alternative solution would be to utilize silicon gate technology and "field shields".

CONCLUSIONS

MOS devices, which historically have been thought of as low voltage logic elements, are capable of operating at high voltages. Such operation is always achieved by incorporating in series with the active channel region a drift region which largely supports the applied voltage. This technique is exactly analogous to the lightly doped collector region used in modern bipolar transistors. Such high voltage MOS devices can be functionally integrated with other components. Output transistors of the general type shown in Fig. 1 have been shown capable of reaching 500 volt drain breakdown voltages and a 1000 volt capability seems possible. More general purpose devices, like the technology of Fig. 2 will have a more limited voltage capabil-

ity because of high fields across gate oxides, very thick epitaxial layers and their consequent isolation problems, and because of parasitic bulk and surface devices. Practical junction isolated circuits appear to be limited to about 200 volts. Dielectric isolation techniques will improve this figure because all of the above problems are eliminated by this technology except the need in transmission gate type applications for high gate oxide fields.

ACKNOWLEDGEMENT

The author wishes to acknowledge valuable discussions with his colleagues at Stanford, particularly S. C. Sun and R. Blanchard.

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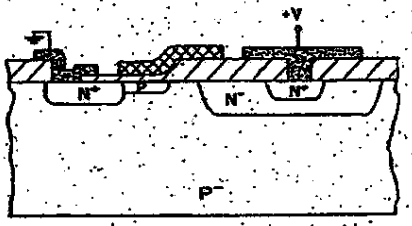

Fig. 1. Schematic cross-section of a high voltage output MOS transistor compatible with low voltage NMOS or DMOS circuits.

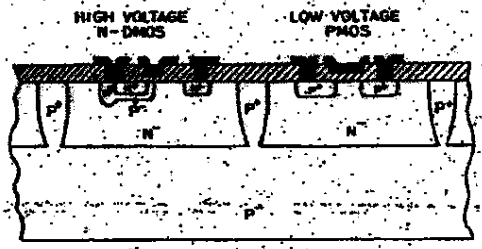

Fig. 2. Cross-section of general purpose high voltage technology based upon thick epitaxial layers and lateral DMOS devices.

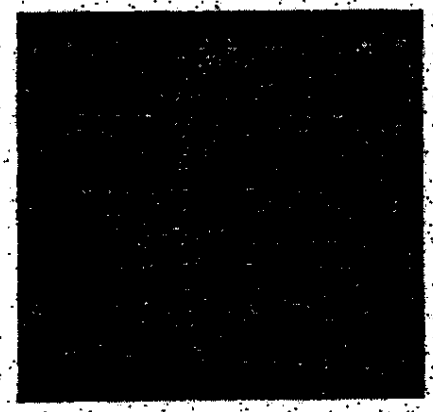

Fig. 3. Photomicrograph of integrated circuit fabricated with the technology of Fig. 2.

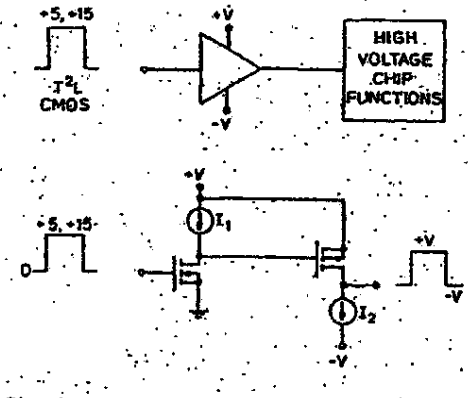

Fig. 4. Basic level shifting function in high voltage ICs and its conceptual realization.

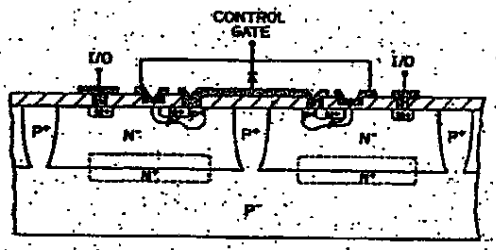

Fig. 6. Cross-section of high voltage symmetrical analog switch using back-to-back DMOS devices.

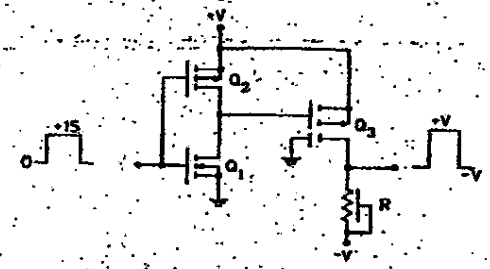

Fig. 5. Practical implementation of the level shift function.
a. circuit schematic
b. photomicrograph of actual realization

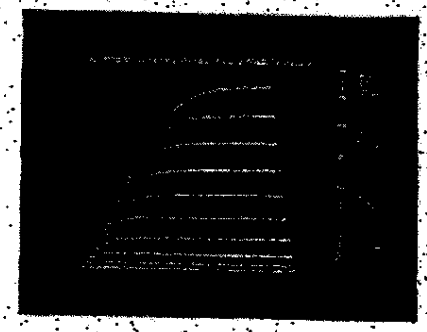

Fig. 7. I-V characteristics at low V_{DS} of the analog switch in Fig. 6.

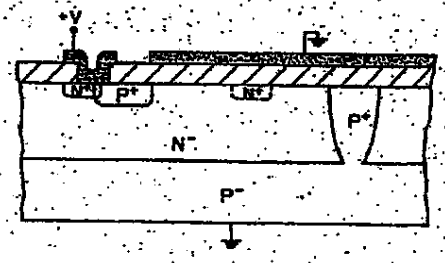

Fig. 8. Surface inversion problem in high voltage ICs. The use of N^+ guard rings is often not possible.

DX 617

SESSION III: SOLID-STATE DEVICES

WAM 3.6: 400V MOS IC for EL Display

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A NUMBER of MOS developments have been attempted to provide operation at voltages higher than 200V[1-5]. Among these, DSA[6] MOST seems to have a promising future. This paper will describe a high voltage, DSA MOS IC which operates in excess of 400V. It was designed as a driver for electroluminescent displays[7]. Low voltage logic and thirty-two high-voltage output transistors are integrated on a single chip. The device consists of a pair of layers patterned as concentric conductive annular strips above which a layer of metal with a circular gap is deposited. This configuration and final passivation over the metal layer permit encapsulation in a plastic package. The high voltage DSA MOST was proposed earlier with a π substrate, a Diffusion-Self-Aligned structure, lightly doped drift region(N^-), and a field plate extended from the drain electrode[1]. The drift region of this device was not covered by field plates; i.e., an offset gate structure. If the field plate is extended to cover all of the drift region in these devices, the electric field at the edge of the drift region will be enhanced and the breakdown voltage reduced.

Figure 1 shows a cutway view of high-voltage DSA MOST and Figure 2 the $V_D - I_D$ characteristics. The main feature of the device is that the drift region is, as a whole, covered by multilayer field plates which consist of two conductive plates extending from the drain and source electrodes, and double-layered floating plates. Because a multiplicity of these floating field plates reduces the electric field enhancement, the structure does little to affect the high voltage characteristics of the offset gate MOST. The offset gate MOST should be hermetically encapsulated to prevent degradation of the device characteristics affected by moisture and/or ionic contamination. The lifetime on-resistance increase by 10% at various temperatures in earlier devices is shown in Figure 3; a comparison between hermetic seal and plastic packages is also indicated. Though the lifetime of the hermetically sealed device is longer than that of the plastic-packaged device by a factor of six, its reliability is poor.

Results of bias aging are shown in Figure 4. The changes of R_{ON} and I_{DS} in the device characteristics are small and the breakdown voltages at V_{GS} = 5V (duty cycle = 0.1%) always exceed 400V. The plastic-packaged device surpassed the results of earlier packaged devices; Figure 3. The plastic-packaged device has some advantages; for example, its cost could be made low and the discharge between a bonding wire and the die edge is eliminated.

High-voltage monolithic integrated circuits for electroluminescent graphic display drivers have also been designed. A block diagram and photomicrograph of a 32b high-voltage MOS IC are shown in Figures 5 and 6, respectively. The logic circuits contain a 32b serial-in/parallel-out shift register, latch and gate circuits. They can operate at a single +5V power supply, and the data I/O interface is TTL compatible. The high-voltage MOST gates are directly controlled by an STB input and $\overline{CL}$ input, even when the shift register is transferring the data.

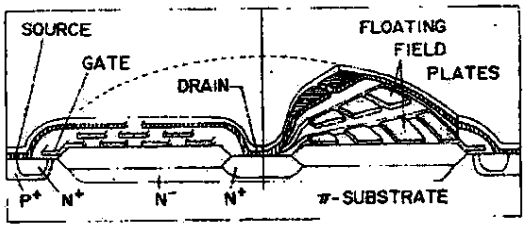

FIGURE 1—Cutway view of the DSA MOSFET.

High Voltage MOSFET	
Drain-Source Breakdown Voltage	400V
ON-Drain Current	50mA
Drain-Source ON Resistance	500Ω
Logic Circuit	
Supply Voltage	+5V
I/O Interface	TTL Compatible
Clock Frequency	dc to 10MHz
Technology	DSA E/D MOS
Chip Size	5.76mm x 3.44mm
Package	42 pin DIP

TABLE 1—Typical characteristics of 32b high-voltage MOS IC.

*Based on concepts of S. A. Arrhenius.

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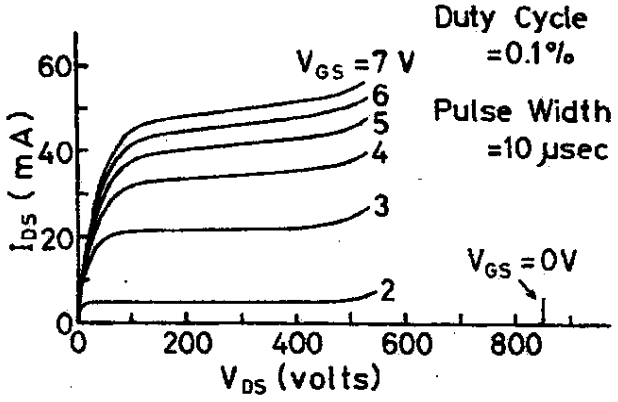

FIGURE 2—I-V characteristics of the DSA-MOSFET.

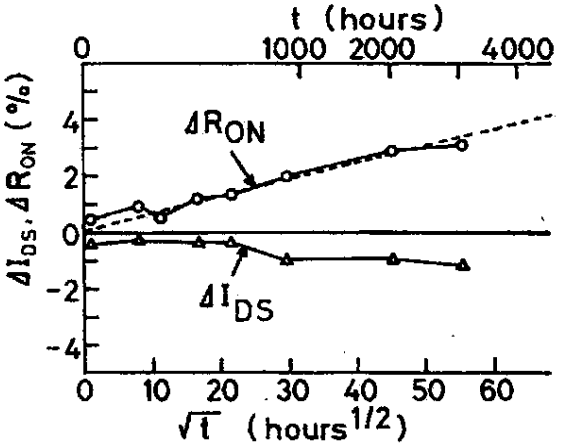

FIGURE 4—The variations of R_{ON}, I_{DS} for 150°C bias test (V_{DS} = 300V, V_{GS} = 0V) in the devices with plastic mold. The lifetime of R_{ON} at 150°C is estimated at 27800 hours by extrapolation.

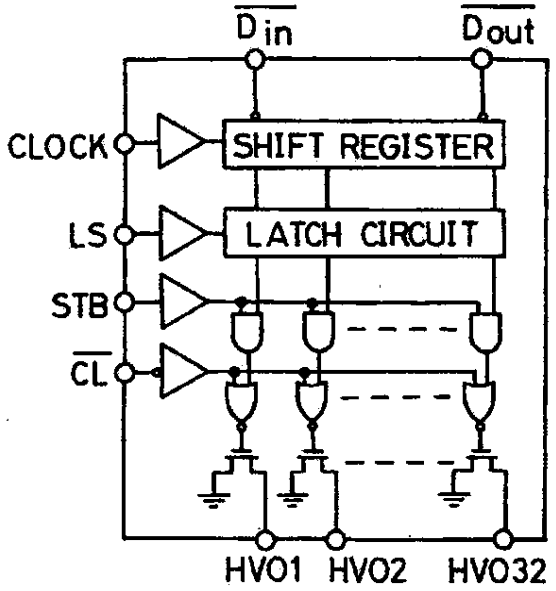

FIGURE 5—Block diagram of the high-voltage MOS IC.

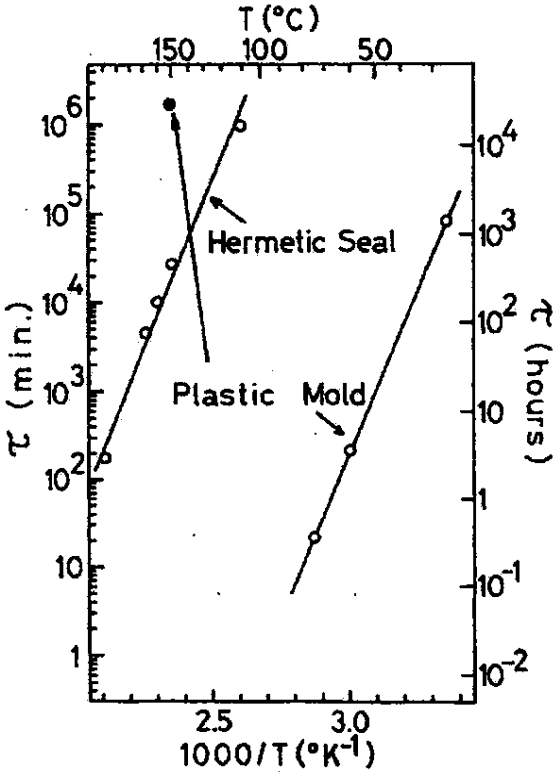

FIGURE 3—Plots of lifetimes of the hermetic seal and the plastic mold in offset device (circle) and that of the plastic mold in the present device (solid dot).* The lifetime for the 300V bias aging is determined by the time required by the increase of the R_{ON} (V_{DS} = 5V, V_{GS} = 5V) of 10%.

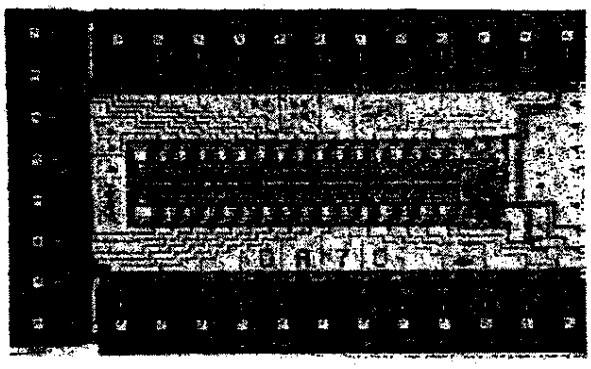

FIGURE 6—Photomicrograph of 32b MOS IC for electroluminescent displays.

DX 618

PROCESS AND DEVICE DESIGN OF A 1000-VOLT MOS IC

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ABSTRACT

High-voltage MOS devices and NMOS logic circuits have been integrated on the same chip by using a silicon-gate isoplanar process that is compatible with present NMOS-LSI technology. The electrical characteristics of a high-voltage MOS device are modeled and characterized in terms of channel length, drift-layer length, drift-layer ion dose, and extended-source field-plate effect. The device structure and the process parameters are optimized to obtain maximum drain saturation current with a low on-resistance and a drain breakdown of 1000 volts. The optimized high-voltage MOS device can perform at a saturation drain current as high as 84 mA with on-resistance as low as 300 Ω within an area of 520 μm × 1320 μm while maintaining a drain breakdown of 1000 volts and drain leakage current less than 30 nA.

INTRODUCTION

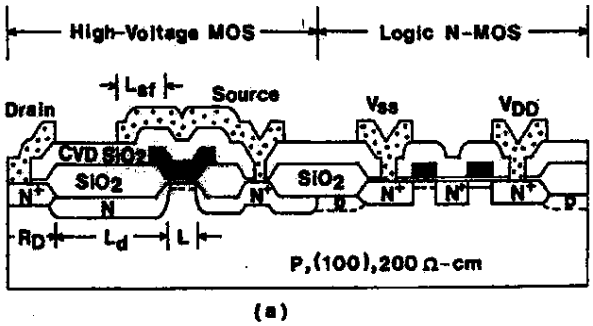
High-voltage MOS integrated circuits are becoming important as driver devices in various display and switching applications. In order to integrate high-voltage MOS devices and logic circuits on the same chip, two different basic approaches have been demonstrated: one uses a vertical MOS structure (1), the other uses a horizontal structure (2-4). In this paper, the authors describe an advanced high-voltage MOS-IC technology that uses a horizontal device structure with a silicon-gate isoplanar process that is compatible with present NMOS-LSI technology. The device structure and the process parameters are optimized to provide a 1000-volt drain-breakdown voltage with maximum drain saturation current and minimum on-resistance.

DEVICE STRUCTURE AND MODEL

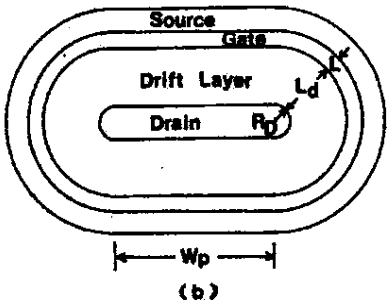
Figure 1(a) shows the cross-section of the high-voltage MOS IC. The high-voltage MOS devices are integrated with NMOS logic circuits on the same chip by using a silicon-gate isoplanar process. The gate electrode of the high-voltage MOS device is driven directly by the output signal of the logic circuit. The high-voltage MOS device has an enclosed structure with an extended-source field plate. Because a recessed-oxide technology is employed in the high-voltage MOS device, the channel region is self aligned not only with the source region but also with the drift-layer region, which in turn is self aligned with the drain region. The logic circuit consists of conventional silicon-gate enhancement- and depletion-mode MOS devices.

Figure 2 shows the schematic model of the high-voltage MOS device. The drain current first increases almost linearly with the drain voltage. The on-resistance is composed of channel resistance and drift-layer resistance. In the case of the race-track pattern shown in Fig. 1(b), the drift-layer resistance R_d is given by

$$R_d = \left[\frac{2\pi q \mu_d N_d}{\ln (1 + L_d/R_D)} + \frac{2q\mu_d N_d W_p}{L_d} \right]^{-1}, \qquad (1)$$



(a)



(b)

Figure 1. (a) High-voltage MOS-IC device structure. (b) High-voltage MOS device pattern.

where N_d represents the total mobile-carrier density in the drift layer. If it is assumed that the drift layer has a uniform impurity distribution and is reverse biased by a drain voltage V_{DS} and a substrate voltage V_{SB}, then N_d is given by

$$N_d = N_{d0} - \frac{N_{d0}}{X_{jd}} \left[\frac{2\epsilon_0 \epsilon_{si}(V_{DS} + V_{SB})}{q} \frac{N_{SB} X_{jd}}{N_{d0}} \frac{1}{(N_{SB} + N_{d0}/X_{jd})} \right]^{1/2}, \qquad (2)$$

where N_{d0} is the total ion dose implanted into the drift layer and X_{jd} is the junction depth of the drift layer. As the drain voltage is increased, the channel region close to the drift layer (p_1) is pinched off as shown in Fig. 2(b).

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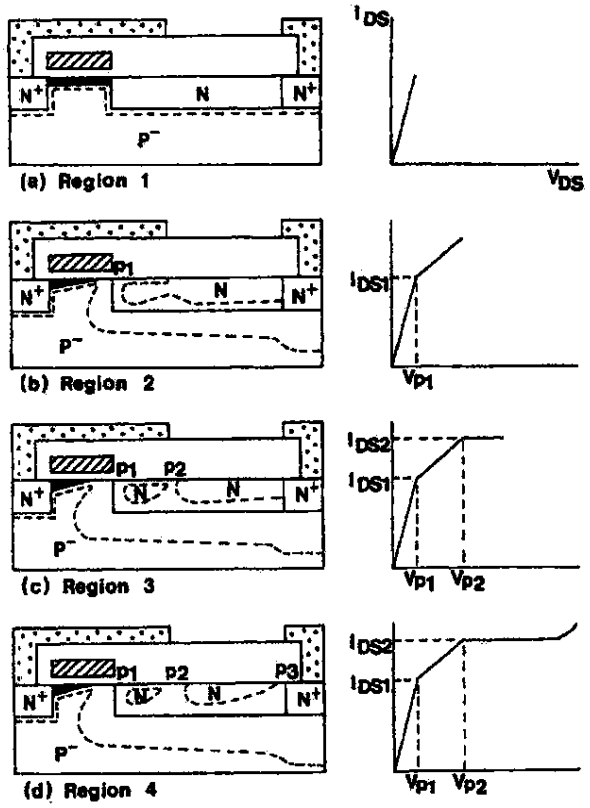

Figure 2. Schematic of high-voltage MOS device model.

When the drain voltage is further increased, the increased drain voltage is dropped across the first pinch-off region. This voltage drop causes channel-length modulation and increases drain current. At the drain voltage of V_{p2}, the region p_2 is pinched off before the surface electric field in the first pinch-off region reaches a critical avalanche electric field ($\cong 3 \times 10^5$ V/cm). Once the region p_2 is pinched off, the increased drain voltage is dropped across the second pinch-off region and is no longer applied to the first pinch-off region. Therefore, the electric field in the first pinch-off region no longer increases. As a result, the surface avalanche breakdown happening at the first pinch-off region can be prevented; furthermore, the channel-length modulation no longer progresses. Therefore, the drain current saturates completely at the second pinch-off voltage. The second pinch-off voltage V_{p2} is given by

$$V_{p2} = V_{p20} + I_{DS2}R_{d2}, \tag{3}$$

where R_{d2} is the drift-layer resistance at the drain voltage of V_{p2}, and V_{p20} is the pinch-off voltage of the drift layer at zero gate voltage. V_{p20} is given by

$$V_{p20} = \frac{q(N_{SB} + N_{d0}/X_{jd})}{2\epsilon_0\epsilon_{si}} \left\{ \left[X_{jd} + \frac{\epsilon_{si}}{\epsilon_{ox}} T_F \frac{N_{SB}X_{jd}}{N_{d0}} + X_{jd}^2 + 2\frac{\epsilon_{si}}{\epsilon_{ox}} T_F X_{jd} \right]^{1/2} - \left(X_{jd} + \frac{\epsilon_{si}}{\epsilon_{ox}} T_F \right) \left(\frac{N_{SB}X_{jd}}{N_{d0}} \right)^{1/2} \right\}^2. \tag{4}$$

When the drain voltage is further increased, finally the region p_3 close to the N^+ drain junction is pinched off. For the same reason mentioned before, this third pinch-off region sustains the drain-voltage increase until the surface avalanche breakdown occurs at the third pinch-off region or until the bulk junction breakdown takes place.

WAFER PROCESS

The starting material is p-type bulk silicon with <100> surface orientation and 200 Ω-cm resistivity. The first step is to grow a thin SiO_2 film followed by a chemical-vapor deposition of Si_3N_4 and SiO_2 films. The source and drift-layer regions are patterned at the same time in a CVD SiO_2 film and a Si_3N_4 film. Phosphorus ions are then implanted into the drift-layer region. Arsenic ion implantation is done for the source region using a photoresist as a masking material. After these two ion-implantation steps, the arsenic and phosphorus impurities are diffused. The active device regions of the logic circuits are then defined in the Si_3N_4 film that was deposited initially. Boron ions are implanted into the field regions of the logic devices. After the field-boron-ion implantation, a thick SiO_2 film is grown selectively in the source and drift-layer regions of the high-voltage MOS device and in the field region of the logic devices. The rest of the process steps are the same as for conventional silicon-gate NMOS LSIs.

EXPERIMENTAL RESULTS

In order to investigate the electrical characteristics of the high-voltage MOS device, the drift-layer ion dose was varied from 4×10^{11} cm^{-2} to 2×10^{12} cm^{-2}. The channel and drift-layer lengths were also ranged from 6 to 16 μm and from 50 to 200 μm, respectively. The gate-oxide and field-oxide thicknesses between the extended-source field plate and the drift layer were 1050 Å and 2.0 μm. In this experiment, a circle pattern with a drain radius of 50 μm was used for the high-voltage MOS device.

Figure 3 shows the typical drain characteristics of a high-voltage MOS device. The drain-breakdown voltage at zero gate-bias voltage is greater than 1000 volts with drain leakage current less than 30 nA. At a gate bias of 4 volts, no surface avalanche current was observed for drain voltages up to 800 volts. The drain-breakdown voltage showed a maximum value at the drift-layer ion dose of 1×10^{12} cm^{-2} and was larger as the drift-layer length was lengthened. As shown in Fig. 4, there is a significant difference in breakdown voltage—approximately 200 to 250 volts—between the two devices; one has an extended-source field plate of 30 μm and the other has none. This difference is due to the existence of a second pinch-off voltage.

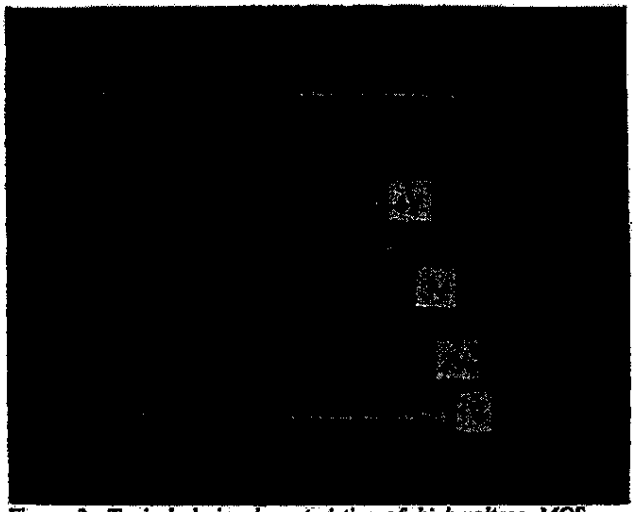

Figure 3. Typical drain characteristics of high-voltage MOS device.

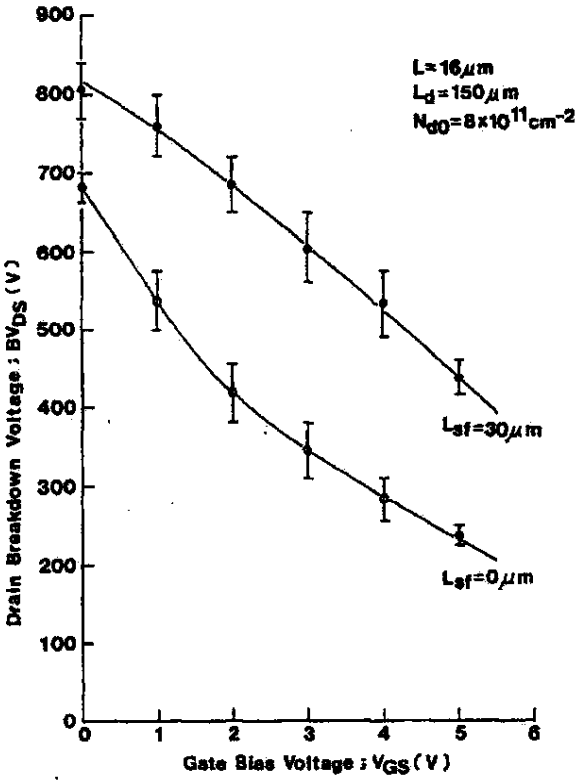

Figure 4. Extended-source field-plate effect on drain-breakdown voltage.

The drain punchthrough current is a strong function of channel length, impurity concentration in the channel region, and drift-layer ion dose. This punchthrough current can be suppressed if the second pinch-off occurs before the potential barrier in the channel region is lowered. Therefore, the higher impurity concentration in the channel region or the lower ion dose in the drift layer allows the shorter channel length without punchthrough leakage current. As shown in Fig. 5, the punchthrough leakage current was controlled to less than 30 nA in the 6-μm channel device with the p-type region surrounding the source area. The surface concentration of this p-type region was 1×10^{16} cm^{-3}. At the drift-layer ion dose of 6×10^{11} cm^{-2}, the punchthrough leakage current was also less than 30 nA in the 11-μm channel device without the p-type region. (See Fig. 6.) However, in this case, the drain-breakdown voltage at zero gate-bias voltage was limited at 650 volts.

The on-resistance, saturation drain current, and pinch-off voltage dependences on channel length, drift-layer length, and drift-layer ion dose have been explained already in other literature (5) as well as by theoretical calculations.

OPTIMUM DEVICE STRUCTURE

In order to maximize the saturation drain current capability while maintaining a 1000-volt drain breakdown, the channel length must be minimized by keeping the drift-layer ion dose at 1×10^{12} cm^{-2}. However, the shorter channel length and the higher drift-layer ion dose result in larger drain punchthrough leakage current. It was shown in Figs. 5 and 6 that either the additional p-type region surrounding the source region or the lower drift-layer ion dose effectively prevented the punchthrough leakage current. On the other hand, the higher drift-layer ion dose is necessary in order to obtain low on-resistance. The

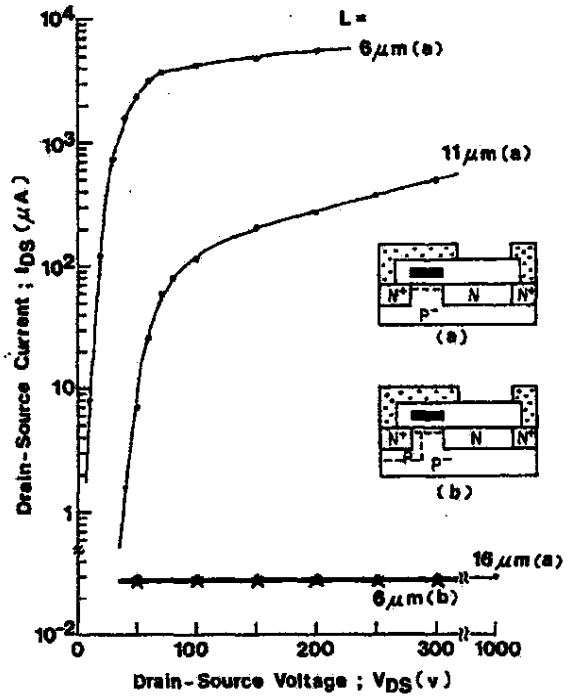

Figure 5. Drain leakage currents for different channel-length devices.
(a); ——●—— *(b).*

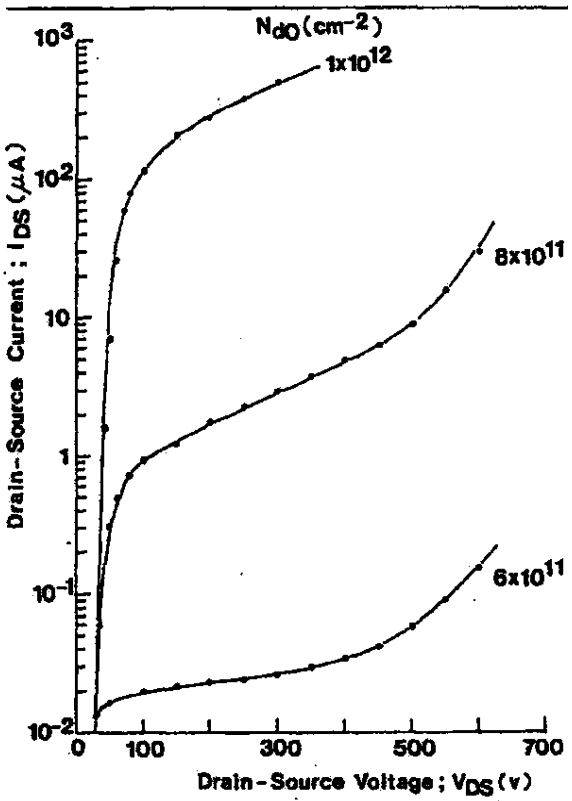

Figure 6. Drain leakage current dependence on drift-layer ion dose.

optimized high-voltage MOS-device structure shown in Fig. 7 takes these factors into account to obtain the maximum drain-current capability with low on-resistance while maintaining a 1000-volt drain breakdown. The source region is surrounded by an additional p-type region that has a surface-impurity concentration of 1×10^{16} cm^{-3}. The gate-threshold voltage is adjusted at 1.0 volt by a channel boron-ion implantation. The drift layer is composed of two regions, N_{d1} and N_{d2}. N_{d1} has an ion dose of 6×10^{11} cm^{-2}. This lightly doped first drift-layer region provides a low second pinch-off voltage to suppress the punchthrough leakage current. The second drift-layer region N_{d2} has an ion dose of 1×10^{12} cm^{-2}, which provides the maximum drain-breakdown voltage and reduces the on-resistance. The optimized high-voltage MOS device, which had a circle pattern with $R_D = 50$ μm, $L = 6$ μm, and $L_d = 200$ μm, demonstrated drain-breakdown voltage as high as 1000 volts with drain leakage current less than 30 nA, on-resistance of 1700 Ω, and saturation drain current of 260 mA/cm at a 5-volt gate bias. In this device, on-resistance can be reduced to 300 Ω by using a race-track pattern.

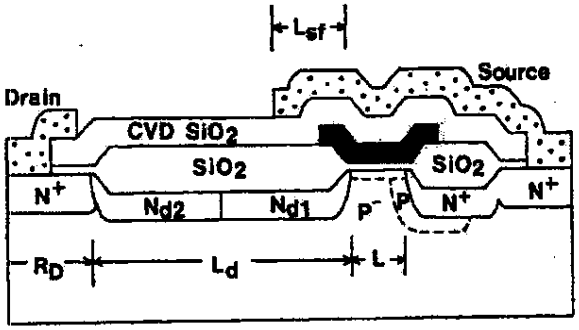

Figure 7. Optimized high-voltage MOS-device structure.

CONCLUSIONS

High-voltage MOS devices and NMOS logic circuits have been integrated on the same chip by using a silicon-gate isoplanar process that is compatible with present NMOS-LSI technology. The electrical characteristics of the high-voltage MOS device were modeled and characterized in terms of channel length, drift-layer length, drift-layer ion dose, and extended-source field-plate effect. It was concluded that the optimum high-voltage MOS-device structure uses a p-type region surrounding a source region with a double drift-layer structure in order to obtain the maximum drain-current capability with a low on-resistance while maintaining a 1000-volt drain breakdown. The optimized high-voltage MOS device achieved drain-breakdown voltage as high as 1000 volts with drain leakage current less than 30 nA, on-resistance as low as 300 Ω, and saturation drain current up to 84 mA within an area of 520 μm × 1320 μm.

ACKNOWLEDGMENTS

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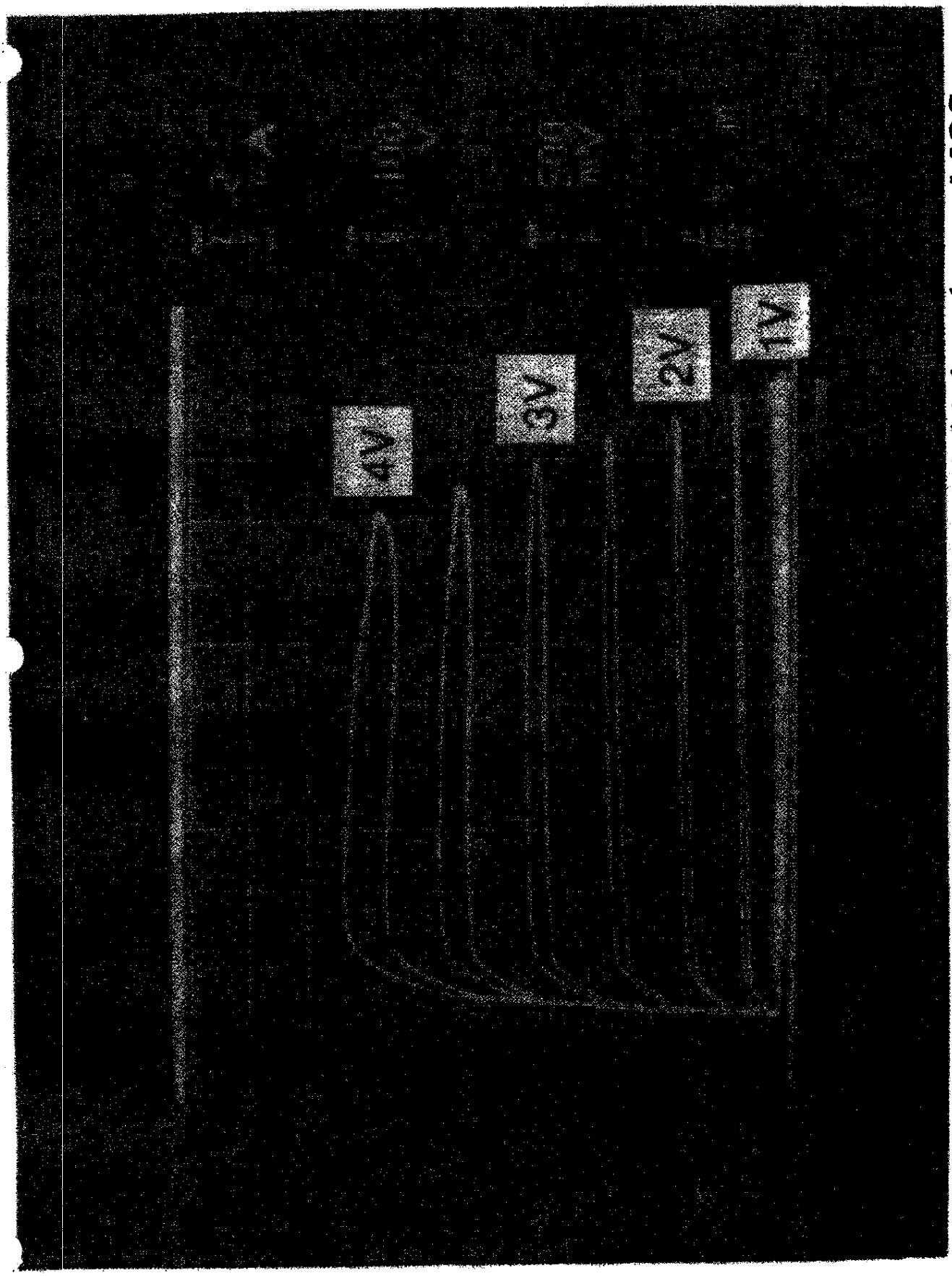

Figure 3. Typical drain characteristics of high-voltage MOS device.

DX 619

INTEGRATED CIRCUITS FOR THE CONTROL OF HIGH POWER

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INTRODUCTION

Vertical power devices are being used in a new class of integrated circuits for the control of high power (1). These vertical devices offer substantial improvements over the traditional planar devices used in linear technology. In the new devices one high current contact (collector or drain) is located on the back of the die which allows a high degree of symmetry in the layout of the base/gate and emitter/source contacts and metal on the front surface. These high current, high power devices are integrated monolithically with a planar IC technology which provides control, interface and protection functions.

The major disadvantages of planar technologies in power control are the interdigitated layout on the surface of the device and resistance associated with the collector contact. The topology of interconnection can cause increased base and emitter/source resistance, and the buried layer generates substantial collector/drain resistance. These fundamental constraints increase the saturation resistance and also make the planar power device more susceptible to hot spot development, limiting the safe operating area in high current operation. The high collector/drain resistance is a very detrimental feature for high current technology. The high drain resistance is particularly noted in high voltage MOS technology (2-5).

In order to obtain higher voltage operation, the planar technology must increase the epi thickness to accommodate the depletion spread into the collector (6-8). These larger thicknesses make it increasingly difficult to provide isolation and deep collector/drain contact diffusions. As a result multilayer epi structures usually are required (7). The extra processing steps add substantially to the process complexity while reducing yield.

Another technology which might be used for power control is the integrated power devices concept. These devices are usually very small scale integrations of a few devices to meet a very narrowly defined function such as an opto-coupled switch (9-10). Such devices do not have the flexibility of medium to large scale integrated circuits demanded by most power IC applications.

Figure 1 indicates some of the projected markets for power applications. It is obvious that standard IC technology cannot meet the market demand for most of the high volume power control applications. These markets can be addressed by the new power control technologies with vertical power devices. These power devices are capable of dissipating 100 watts and controlling switched loads of 300 to 400 watts. The output device is generally capable of a minimum breakdown voltage of about 100 volts.

At Motorola the technologies are generically known as SMARTpower™. Other companies have also been engaged in the development of such technology. For example, National has produced the STEEL™ line of voltage regulators using a vertical output device integrated with conventional linear IC planar technology (11). Many other companies have been pursuing the power control market. Among them are International Rectifier, General Electric, Siemens, Texas Instruments, Mitsubishi, Lambda, Harris and others. Some of these efforts are summarized in Table 1.

HIGH POWER TECHNOLOGY

Figure 2 shows the cross section of the Motorola SMARTpower I technology. Many of the features of power control IC technology are evident. It can be seen that the PNP power device is vertical, with the collector on the back of the die. A low resistivity substrate is utilized with the standard power transistor back metallization. The collector resistance of a 15 ampere device is approximately 70 milliohms.

Some form of isolation is necessary between the power device and the control section. The N-epitaxial layer in which the CMOS is built must be at the most positive potential of the circuit to eliminate forward biasing of the vertical collector into the control circuit. This can be achieved by a conventional isolation diffusion or by some other means such as a moat or an electrical short having the effect of placing a high value resistor between the emitter and base of the PNP power device.

The control section is metal gate CMOS. CMOS is a self-isolating technology which does not need vertical or latteral isolation. One of the principle advantages of metal gate CMOS is manufacturability. Another is the ease with which the CMOS process merges with the PNP epi base power transistor

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process. Also, a quality capacitor is inherent in the process, an important factor in linear circuit design.

A variety of active devices are available for circuit design. There are four basic MOS transistors, a high and low voltage FET of both N and P channel type. The high voltage NMOS devices have a drain breakdown exceeding 45 volts and the P channel devices exceeding 60 volts. The high breakdown voltage is achieved by the use of lightly doped drain diffusions. The P well parasitic NPN transistor has a breakdown voltage exceeding 40V and a beta typically between 200 and 400. A large variety of resistors are available between the N-, N+, P- and P+ diffusions together with the P well. The large number of diffusions also allow the construction of a variety of different avalanche diodes.

The power device has benefitted by the application of modern fine-line photolithography. The design rules which are used in the SMARTpower I technology have not been very aggressive but still are smaller than typical power discrete design rules by an order of magnitude. As a result, the SMARTpower PNP transistor reflects this capability. Its saturation voltage is a factor of 2 times lower, at high currents, than the equivalent discrete device. The F-tau of these devices is between 3 and 5 times higher than devices with equivalent base widths. The device has a somewhat smaller SOA than a standard epi base power device (see Figure 3), but this characteristic may be improved without serious compromise by judicious use of lumped ballasting.

OTHER POWER CONTROL VARIATIONS

The combination of PNP and CMOS was observed by Anthony New to have compatible doping and profiles which merge reasonably well. This suggested the original SMARTpower I technology. The inverted technology, NPN with CMOS is substantially more complex. There are generally two ways to achieve the end result. The first way is to use, much like SMARTpower I, a P-epi layer used as the CMOS substrate and NPN base. To accomodate the lightly doped N well, this epi layer must be very lightly doped. This necessitates some form of twin well technology and some increased complexity in the epi layer to withstand the collector-base breakdown voltage without punch-through. The other method is the use of vertical isolation as used in the National STEEL voltage regulator. The approximate device cross section is shown in Figure 4. The STEEL process uses bipolar control circuits. If CMOS were used instead of bipolar, the cross section would differ only in surface topology and the more limited use of vertical isolation.

Another obvious combination is the integration of an N-channel power MOS device with CMOS. In this case, Figure 4 would be somewhat modified to reflect the power NMOS device merged with the CMOS control. This particular combination is known as SMARTpower II at Motorola. This technology has a great deal of symmetry in the process, and many steps can be shared between the CMOS and the power MOS device. The technology can be described as the "Universal Technology" and is capable of building virtually every active device now commonly used. Indeed, it can build NMOS and PMOS devices of high and low voltage, two different threshold NMOS devices, two different isolatable NPN high voltage transistors, lateral PNP transistors, IIL devices, high voltage DMOS, and power DMOS. A good MOS capacitor, however, requires a separate photomask.

LIMITATIONS OF THE TECHNOLOGY

It can immediately be seen from Figure 2 that there is only one possible collector. This is the major limitation of the power control technology. With a vertical power device there can only be one substrate contact. This limitation is quite substantial. For example, a large market segment which would otherwise be addressed by the SMARTpower technology is the high end audio amplifier market. Efficient amplifiers, however, are not single ended.

Other limitations are the compromises which must be made for the combination of the power device and the IC control. In SMARTpower I the limitation is found in the base width of the PNP. The base must be made wide enough to hold the P-well of the N- channel CMOS without substantially compromising the PNP base transport term and breakdown voltage of the technology. Fortunately a reasonable compromise is possible. In the case of the power NPN or power NMOS there is a trade-off of collector resistance against vertical isolation voltage breakdown.

The power devices have breakdown voltages orders of magnitude higher than the control circuit. To use these high breakdown voltages on the same chip with the lower voltage control circuit requires a low voltage power supply either on-chip or off-chip with the power device to be used in the common source/emitter configuration. If the device is used in a common drain/collector configuration, multiple power output devices are available but the control circuit generally sees the the entire voltage drop.

There are a few things which were thought to be limitations but are not. First, the high gain CMOS operational amplifiers were thought to have large offsets. This is not true, and modest layout care has produced very well matched pairs, exceeding or equalling normal bipolar matching. Contrary to other rumors, the authors have not detected any measurable offset drift due to threshold changes as a result of high temperature operation during power-on life tests. It is suspected that these perfidious tales were invented by bipolar partisans.

THE "SMART" OF SMARTpower

The "smarts" of the technology can be divided into three major functions: control, interface, and protection. Control generally senses some external quantity and adjusts the power device to compensate for any deviation. In a voltage regu-

lator, the external quantity is the output voltage and the internal control is the amount of current supplied to a variable load.

The interface function provides a generalized "level shift" function to receive and transmit control information on a control interface. These sort of functions are represented by the solid state switch.

The last group of "smarts" provide protection for the power device. These circuits monitor the power device to see if it is operating within its temperature and SOA curves and modify its power dissapation accordingly. These functions are not trivial and consume most of the effort in any design.

TOWARD THE FUTURE

The goal for any integration effort is to provide a better function or a cheaper price. In the power control market the major requirement is providing a lower installed cost to the user. The major market is replacement of functions now filled by older technology.

The fluorescent light ballast is an example of an older technology which is being targeted by the new. The market is very large, tens of millions of units a year. The problems are manifold. (Merging IC technology and power control uncovers a multitude of idiosyncracies on both sides of the equation.) Potentially, however, the IC replacement can be less expensive and provide increased function.

Motor control, AC line operation, automotive and transportation applications all are open to the new technology. The applications are wide, the possibilities are endless, however the designer must be eclectic.

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TABLE I
DEVICE TECHNOLOGIES FOR POWER IC's

Generic Name	Output Device	Control Circuit	Isolation	Maximum Voltage	Maximum Current
SMARTpower I	PNP*	CMOS	J.I.	MEDIUM	HIGH
SMARTpower II	TMOS*	CMOS BIPOLAR	J.I.	MEDIUM	HIGH
STEEL(NATIONAL)	NPN*	BIPOLAR	J.I.	LOW	HIGH
INTEGRATED POWER DEVICES (SIEMANS)	TMOS*	NMOS	CMOS P-WELL	HIGH	HIGH
SSSX (IR)	LATERAL THYRISTOR	NMOS	P-WELL	HIGH	HIGH
BIDFET (TI) CMOS-DMOS (MOTO)	PLANAR DMOS	CMOS BIPOLAR	J.I.	MEDIUM	LOW
HV MOS	LATERAL HV MOS	NMOS	GUARD RINGS FIELD PLATES	HIGH	LOW
DIC	MOS BIPOLAR	MOS BIPOLAR	DIELECTRIC ISOLATION	HIGH	MEDIUM
SOS	LATERAL HV MOS	MOS	DIELECTRIC ISOLATION	HIGH	LOW
LINEAR I	BIPOLAR	BIPOLAR	J.I.	LOW	MEDIUM
LINEAR II	BIPOLAR	BIPOLAR	UP ISO J.I.	MEDIUM	MEDIUM

LOW VOLTAGE IS LESS THAN 60 VOLTS, MEDIUM VOLTAGE BETWEEN 60 AND 400 VOLTS, HIGH VOLTAGE IS OVER 400 VOLTS.

LOW CURRENT IS LESS THAN .5 AMP, MEDIUM CURRENT BETWEEN .5 AND 5 AMPS, HIGH CURRENT IS GREATER THAN 5 AMP.

*SIGNIFIES COLLECTOR OR DRAIN CONTACT ON BACK OF DIE.

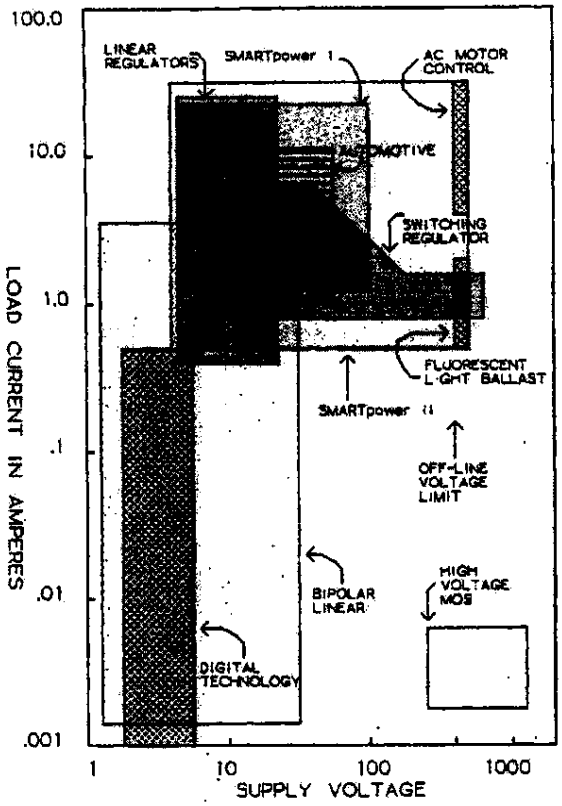

Figure 1. Capability and market overlap for power IC technology.

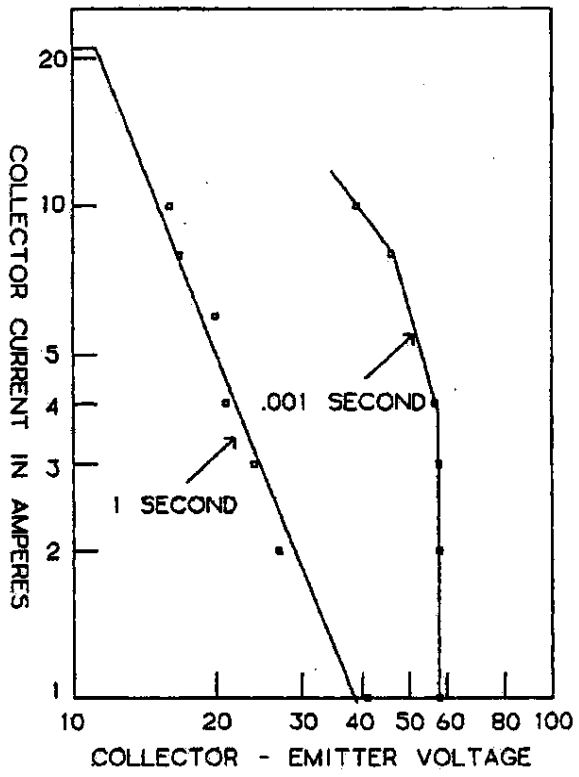

Figure 3. SOA curve of the SMARTpower I PNP output transistor.

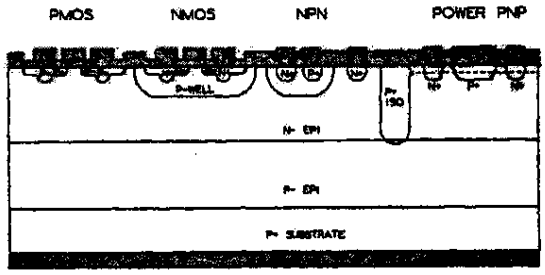

Figure 2. SMARTpower I device cross section.

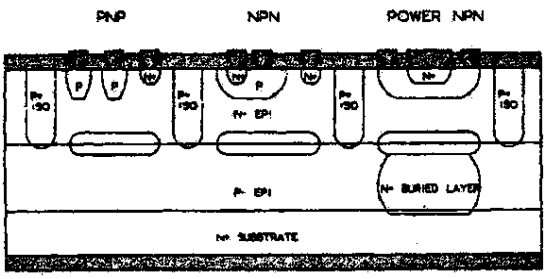

Figure 4. Cross section of the National bipolar STEEL technology (11).

DX 620

INTEGRATED POWER DEVICES

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ABSTRACT

One of the two main trends in the power integration is the combination of logic functions with high voltage output stages resulting in complex HVIC chips which are mainly used for display driving and telecommunication applications. The other trend is to build high current high voltage structures with integrated additional functions making the power devices better compatible to normal IC's and microcomputers.

INTRODUCTION

The rapid advances made in integrated circuit technology have also lead to increased activities in the field of integrated monolithic high-voltage and power systems. The continuing growth in know-how in device physics and the introduction if IC fabrication technologies for complex HV and power systems are the driving forces behind the development of a widening variety of high-voltage and power ICs or functionally integrated structures.

This paper uses the term "power device" as a general description for all those devices which can block higher voltages than "normal, non-power" devices and (but this is not obligatory) which can handle higher currents than the usual devices. The voltage and current limits which "make" a high-voltage device cannot be defined in general terms; the type of technology used also plays a role. While bipolar analog ICs for a 40-V supply voltage can be manufactured easily, for devices in CMOS or NMOS circuits 20 volts is already a high value which cannot be achieved with standard design and processing. Two particular problems arise in the manufacture of power ICs: Firstly, it is not simple to make HV planar p-n junctions with stable and reliable electrical characteristics. Secondly, the usual isolation techniques used for low voltage ICs are not adequate for isolating at high voltages.

The whole problem is complicated still by further additional constraints with respect to cost-effectiveness: a power IC process should preferably be no more complex or expensive than standard processes.

Integrated power devices can be approached in various ways. The application spectrum ranges from HV display driver ICs and telecommunications ICs to optically coupled MOSFET-fired thyristors and triacs switching kilowatts of power.

This paper will attempt to provide an overview of the topic, without claiming in any way to be exhaustive, given the extent of the subject matter.

HV PLANAR P-N JUNCTIONS

A planar p-n junction, i. e. a heavily doped region embedded into the surface of a weakly doped substrate, has both a theoretical and an actual breakdown voltage, the actual breakdown voltage being much lower.

The reasons for this reduction in breakdown voltage, which are well known, are field crowding on the surface due to the extreme curvature of the junction, the surface charge and the moving ions on the outer surface of the oxide.

For planar p-n junctions with breakdown voltages approaching the bulk value, the surface field must be reduced. Two basic approaches have recently been taken up to achieve surface field reduction.

One of them is the field plate structure shown in Fig. 1. It is characterized by a conducting field plate covering a sloping insulating layer surrounding the heavily doped region. The structure is bordered by a channel stopper ring. The structure, for which optimum dimensions can be calculated using two-dimensional modeling, provides under reverse bias a continuously widening space charge layer below the field plate, resulting in the desired surface field reduction. It is a very simple structure and remains absolutely stable due to the perfect shielding of the space charge layer from the moving ions on the top of the structure, but it has the disadvantage of being awkward to fabricate. Simplified versions of the field-plate solution are easy to realize and are widely used in various power devices, as illustrated in Fig. 2.

While a wide variety of field-plated solutions exist, each can be considered a useful approach derived from the basic arrangement in Fig. 1.

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